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62102017	27.04.1987	
62012018	27.04.1987	
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62167537	03.07.1987	
62167538	03.07.1987	
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G03B 41/00

(52) UK CL (Edition K)
G2A ACJ AG1X

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GB 2078383 A US 4641937 A

(58) Field of search
UK CL (Edition K) G2A ACJ ACV ADNX ANJ
INT CL[5] G03B

(71) Applicant
Canon Kabushiki Kaisha

(Incorporated in Japan)

No 3-30-2, Shimomaruko, Ohta-ku, Tokyo, Japan

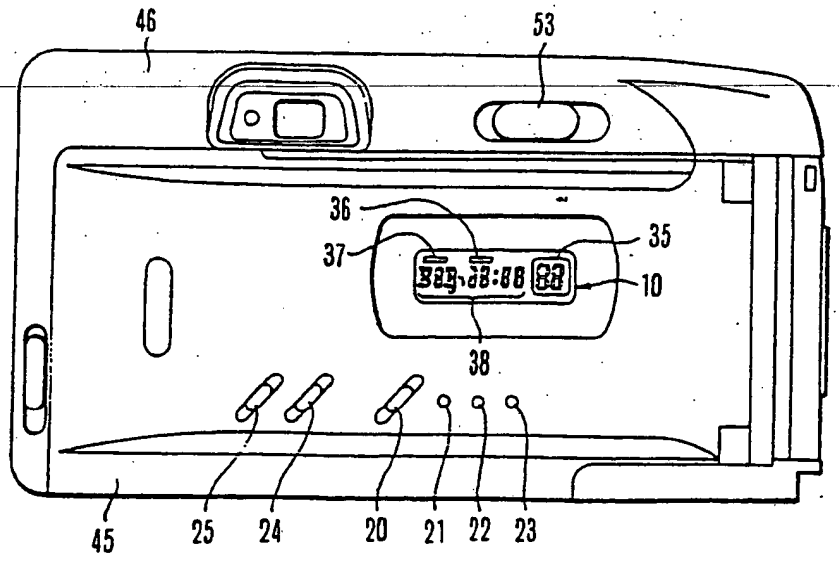
(72) Inventors
Koichi Matsumura
Akira Yoshihara

(74) Agent and/or Address for Service
Sanderson and Co
34 East Stockwell Street, Colchester, Essex, C01 1ST, United Kingdom

(54) Camera and photographic device

(57) A camera arranged for time-lapse photography has a timer for counting time intervals for time-lapse photography. The camera body has a main switch 53, and when that switch is in the OFF state, the timer is prohibited from operating. Also described is a photographic device having this function and arranged for use with a camera.

FIG.1



GB 2 242 753 A

FIG.1

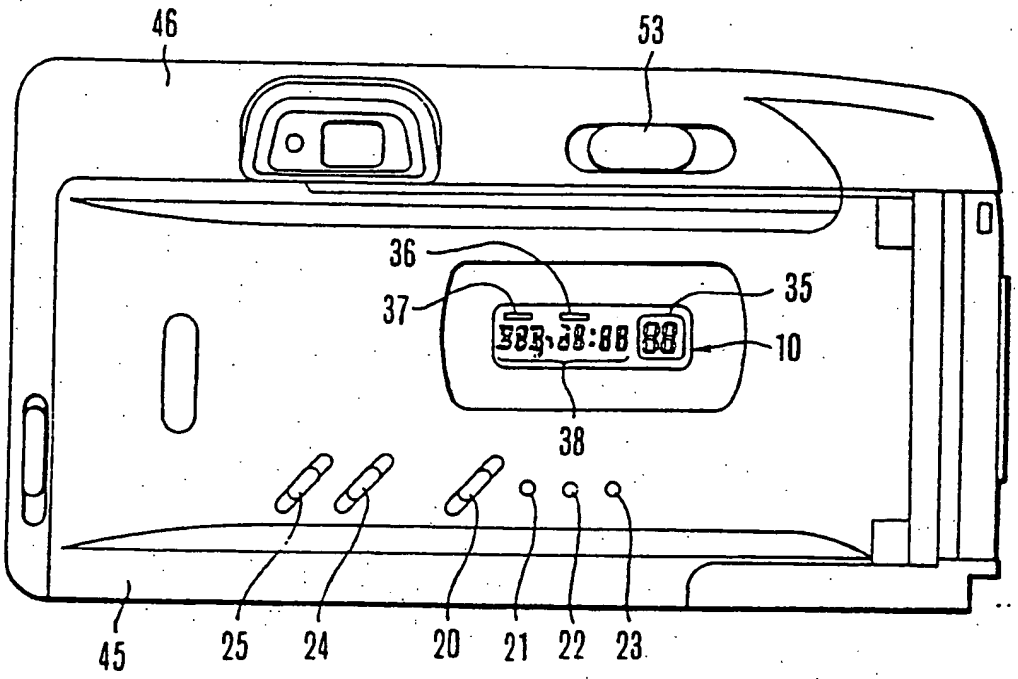


FIG.2

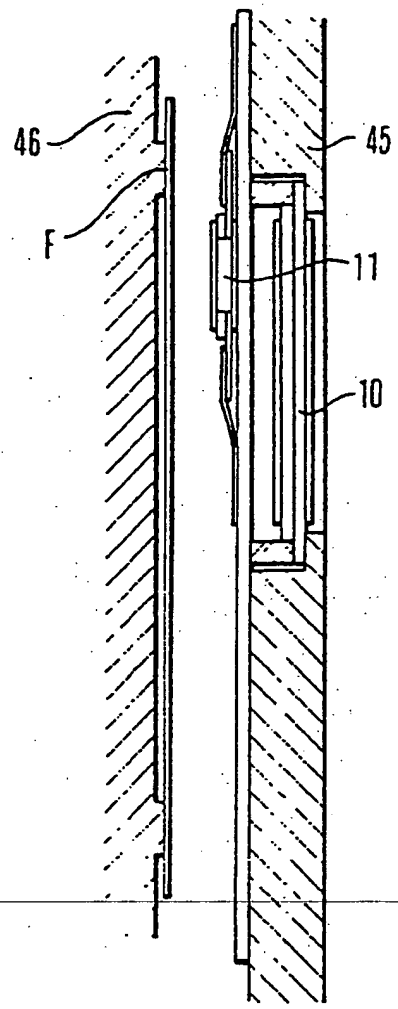


FIG.3

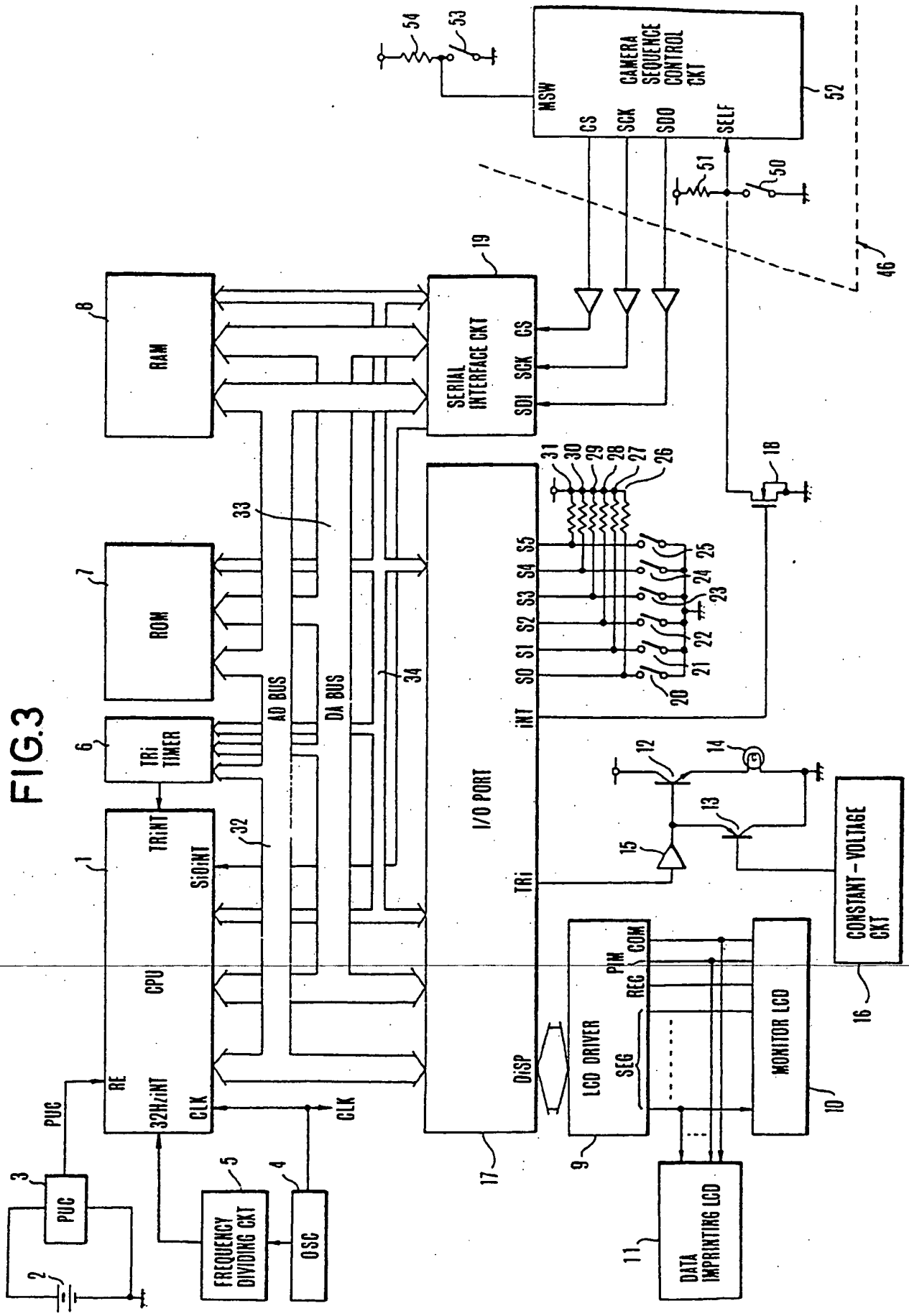

CAMERA SEQUENCE CONTROL CKT
MSW
CS
SCK
SDO
SELF
52
54
53
51
50
46
19
SERIAL INTERFACE CKT
SDI SCK CS
RAM
8
ROM
7
TRi TIMER
6
AD BUS
DA BUS
33
34
I/O PORT
iNT
SO S1 S2 S3 S4 S5
31 30 29 28 27 26
25 24 23 22 21 20
18
12
14
13
15
TRi
CONSTANT-VOLTAGE CKT
16
CPU
TRiINT
SIOiINT
32
RE
32HziINT
CLK
1
PUC
3
2
FREQUENCY DIVIDING CKT
5
OSC
4
CLK
DiSP
LCD DRIVER
PIM
REG
COM
SEG
9
MONITOR LCD
10
DATA IMPRINTING LCD
11
17

FIG.4

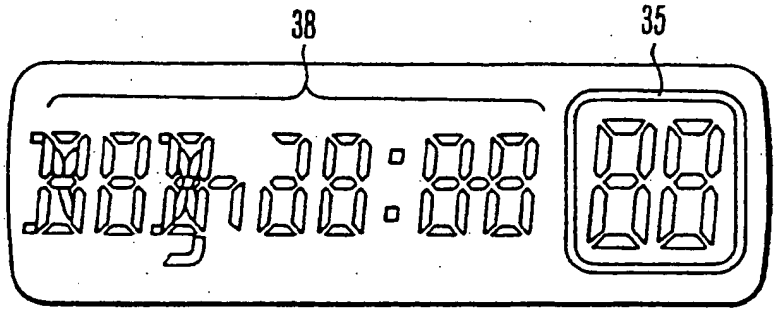


FIG.5

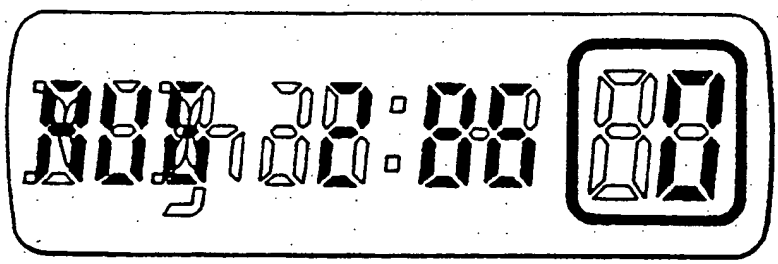


FIG.6

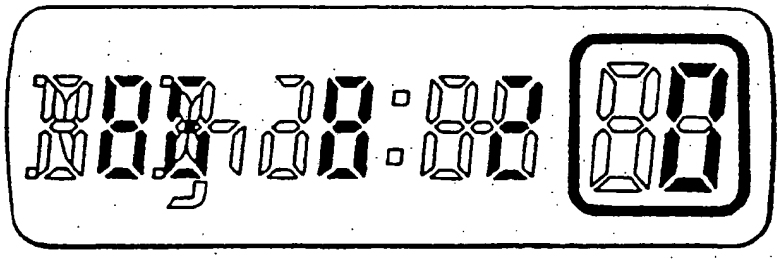


FIG.7

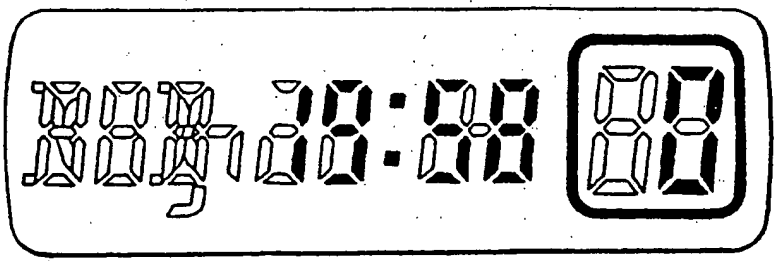


FIG.8

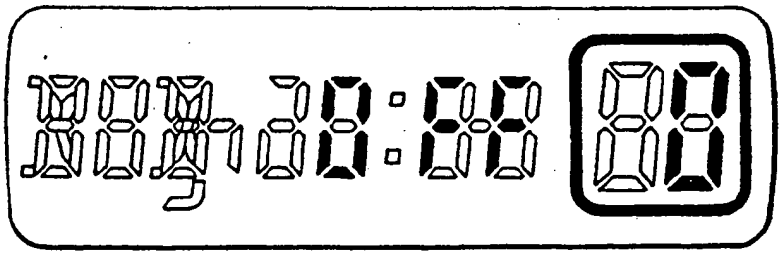


FIG.9

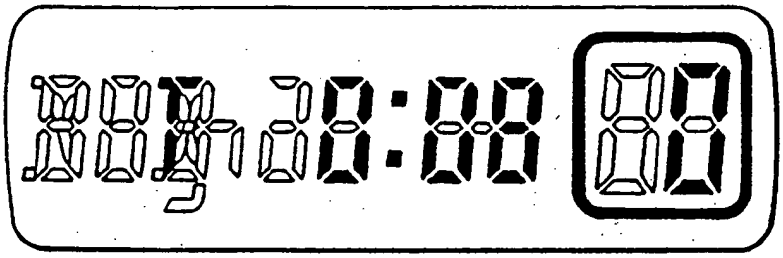


FIG.10

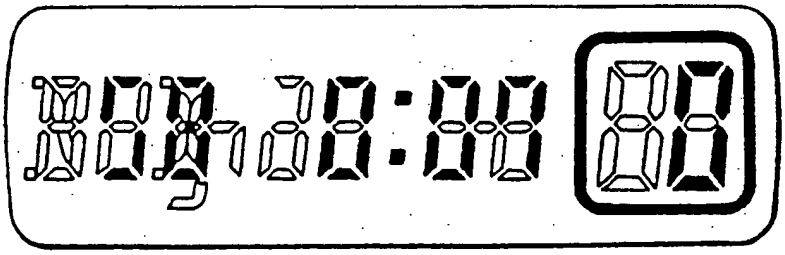


FIG.11

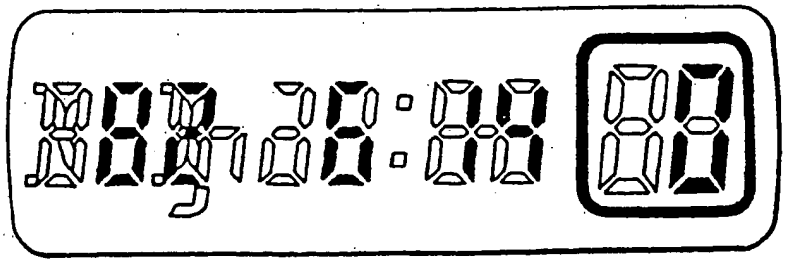


FIG.12

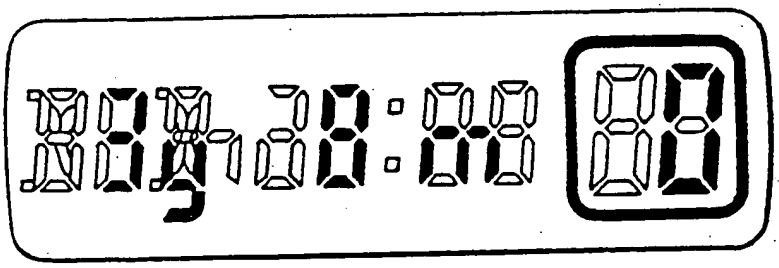


FIG.13

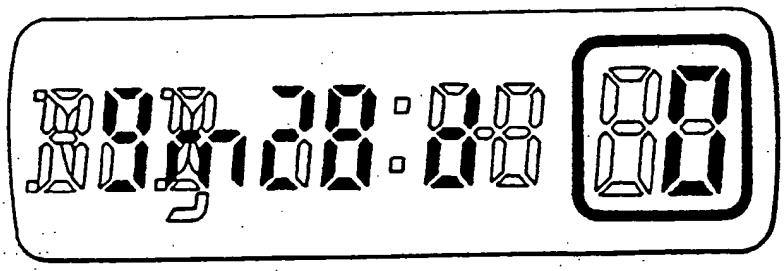


FIG.14

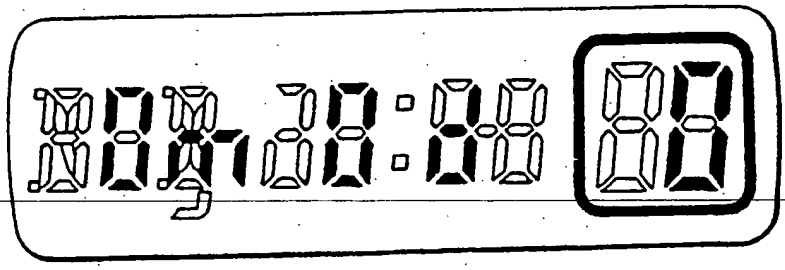


FIG.15A

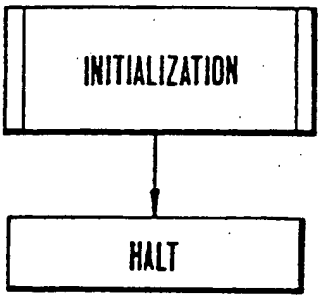


FIG.15B

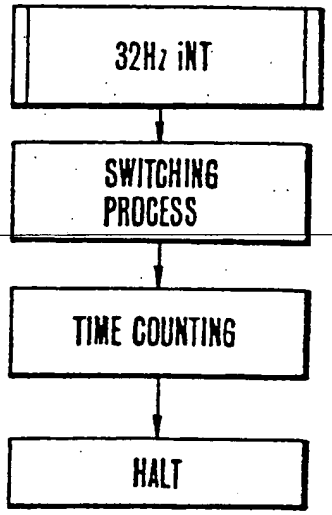


FIG.15C

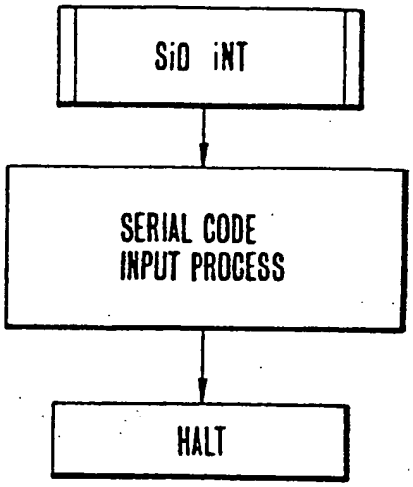


FIG.15D

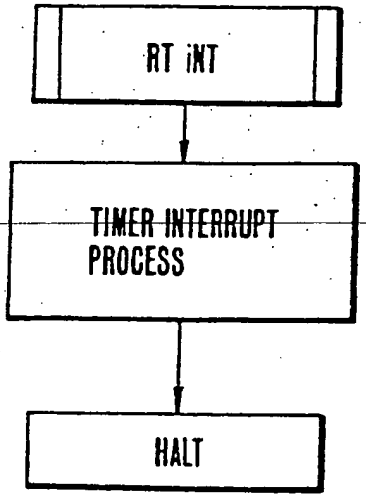


FIG.16A

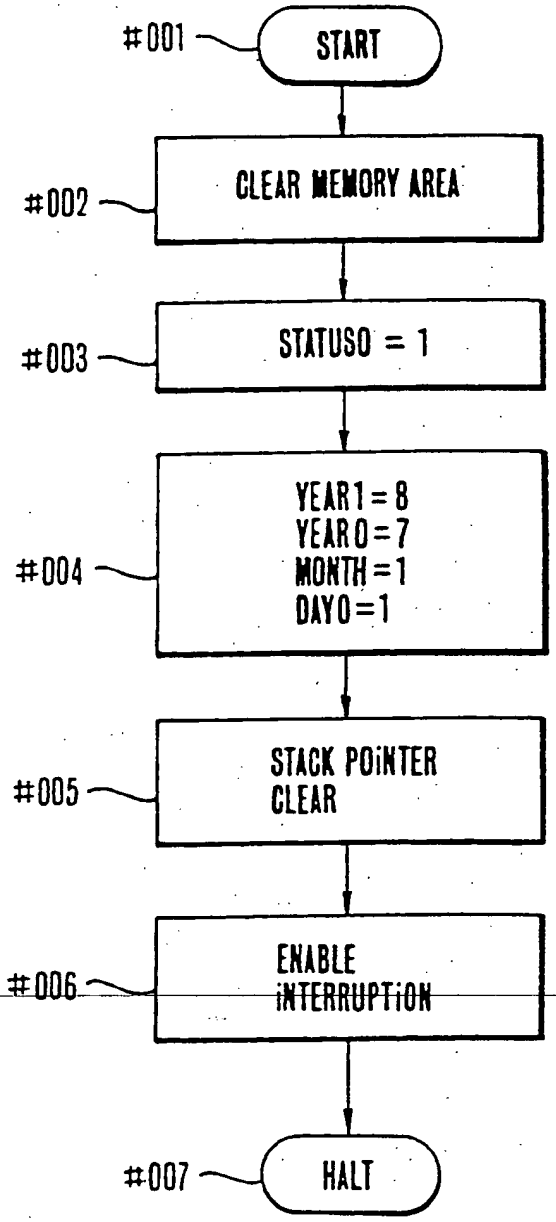

#001
START
#002
CLEAR MEMORY AREA
#003
STATUS0 = 1
#004
YEAR1 = 8
YEAR0 = 7
MONTH = 1
DAY0 = 1
#005
STACK POINTER
CLEAR
#006
ENABLE
INTERRUPTION
#007
HALT

FIG.16B

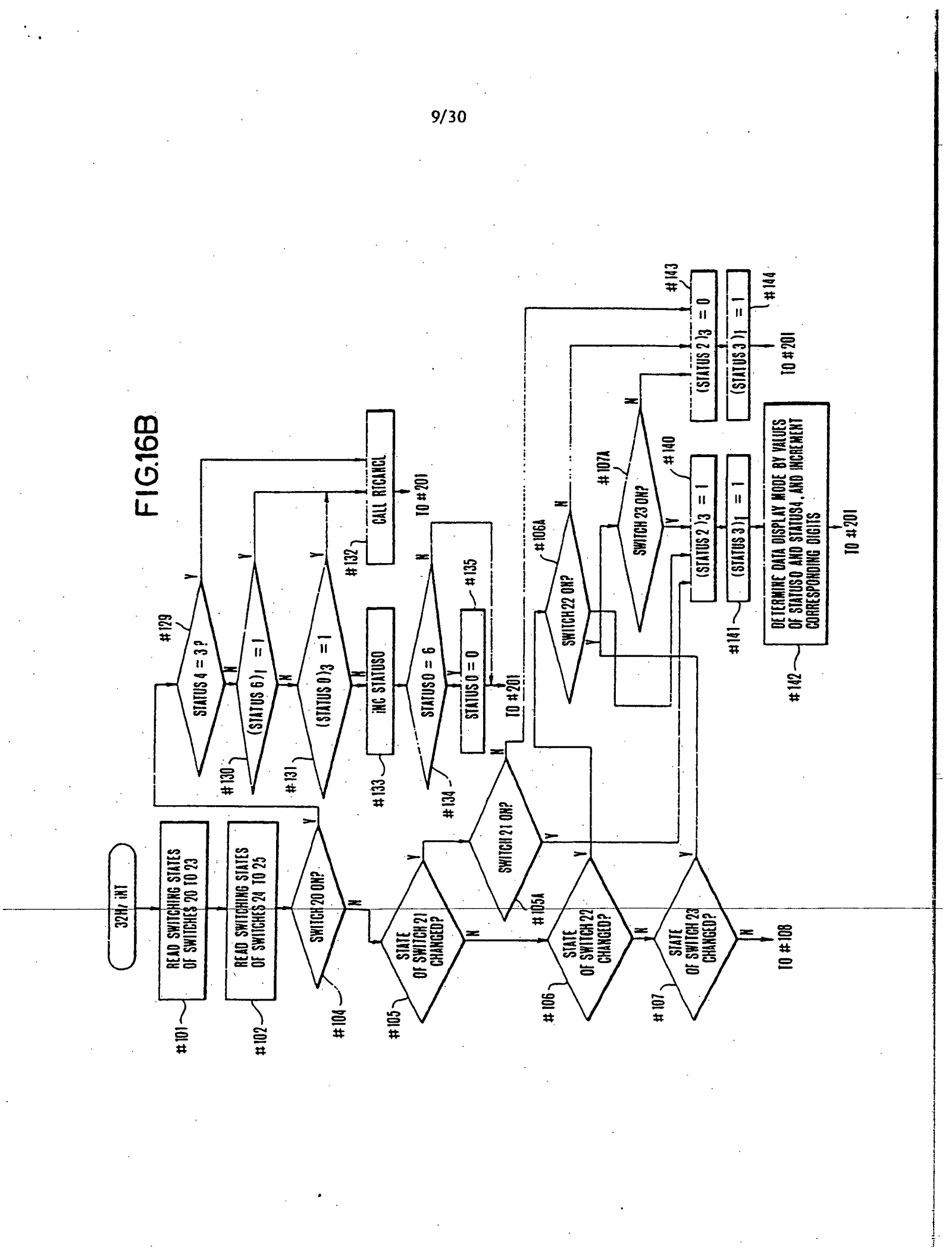

32Hr INT
READ SWITCHING STATES OF SWITCHES 20 TO 23
#101
READ SWITCHING STATES OF SWITCHES 24 TO 25
#102
SWITCH 20 ON?
#104
STATE OF SWITCH 21 CHANGED?
#105
SWITCH 21 ON?
#105A
STATE OF SWITCH 22 CHANGED?
#106
SWITCH 22 ON?
#106A
STATE OF SWITCH 23 CHANGED?
#107
SWITCH 23 ON?
#107A
TO #108
STATUS 4 = 3 ?
#129
(STATUS 6)1 = 1
#130
(STATUS 0)3 = 1
#131
CALL RICANCL
#132
TO #201
INC STATUS0
#133
STATUS 0 = 6
#134
STATUS 0 = 0
#135
TO #201
(STATUS 2)3 = 1
#140
(STATUS 3)1 = 1
#141
DETERMINE DATA DISPLAY MODE BY VALUES OF STATUS0 AND STATUS4, AND INCREMENT CORRESPONDING DIGITS
#142
TO #201
(STATUS 2)3 = 0
#143
(STATUS 3)1 = 1
#144
TO #201
Y
N

FIG.16C

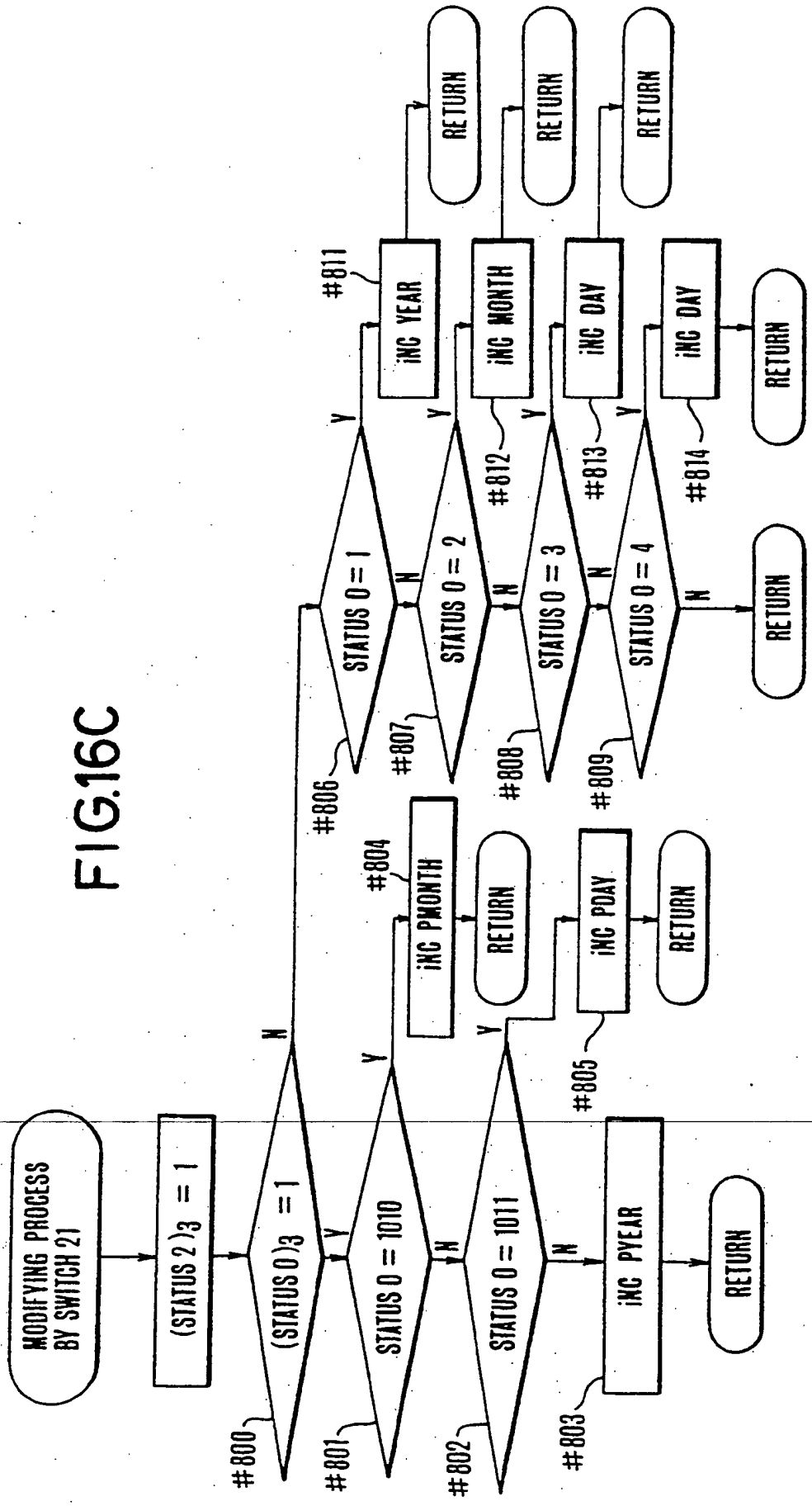

MODIFYING PROCESS BY SWITCH 21
(STATUS 2)3 = 1
(STATUS 0)3 = 1
STATUS 0 = 1010
STATUS 0 = 1011
INC PYEAR
INC PMONTH
INC PDAY
RETURN
#800
#801
#802
#803
#804
#805
STATUS 0 = 1
STATUS 0 = 2
STATUS 0 = 3
STATUS 0 = 4
INC YEAR
INC MONTH
INC DAY
INC DAY
#806
#807
#808
#809
#811
#812
#813
#814
Y
N

FIG.16D

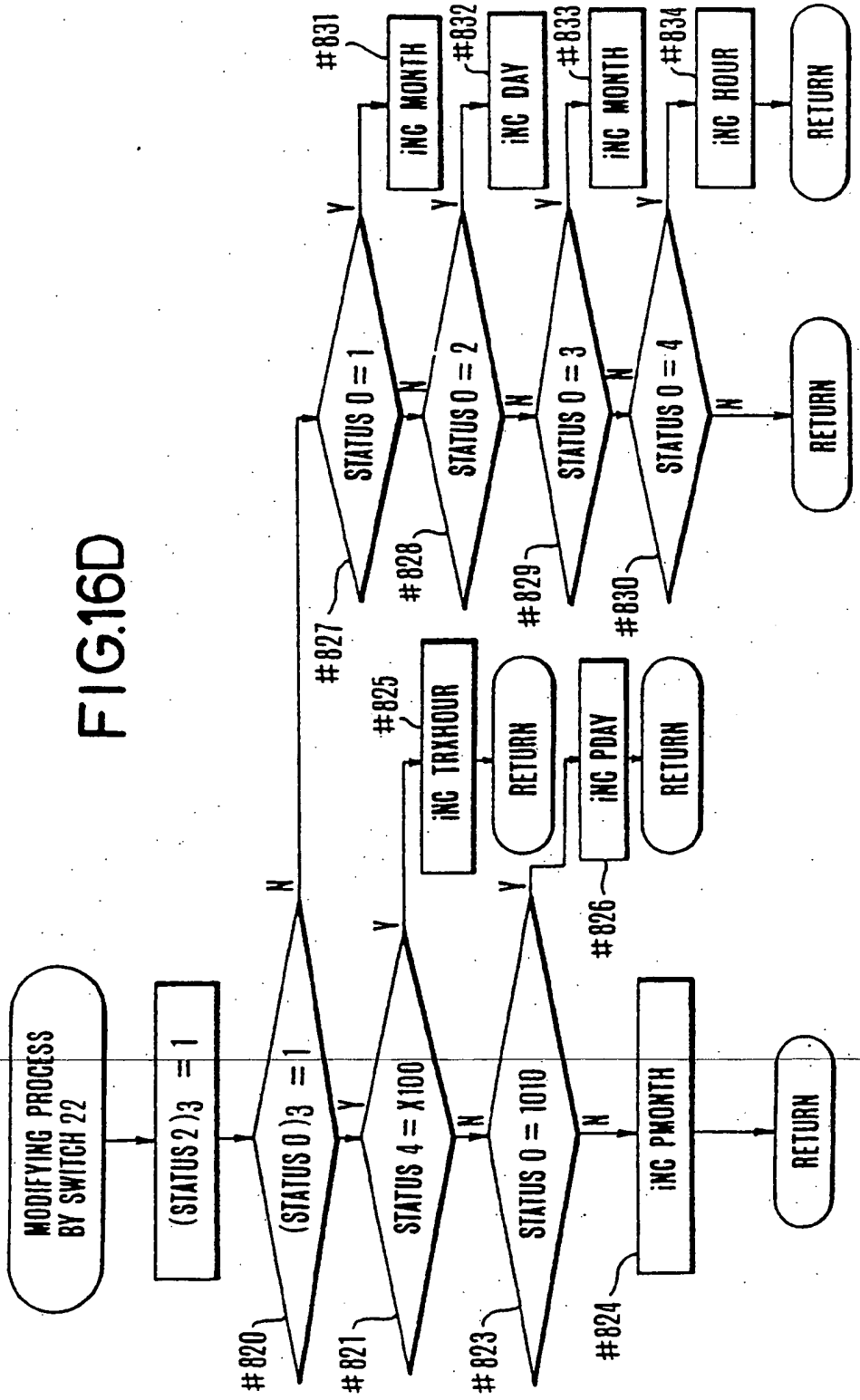

MODIFYING PROCESS BY SWITCH 22
(STATUS 2)3 = 1
(STATUS 0)3 = 1
STATUS 4 = X100
STATUS 0 = 1010
ING PMONTH
RETURN
#820
#821
#823
#824
ING TRXHOUR
RETURN
ING PDAY
RETURN
#825
#826
STATUS 0 = 1
STATUS 0 = 2
STATUS 0 = 3
STATUS 0 = 4
#827
#828
#829
#830
ING MONTH
ING DAY
ING MONTH
ING HOUR
RETURN
#831
#832
#833
#834
Y
N

FIG.16E

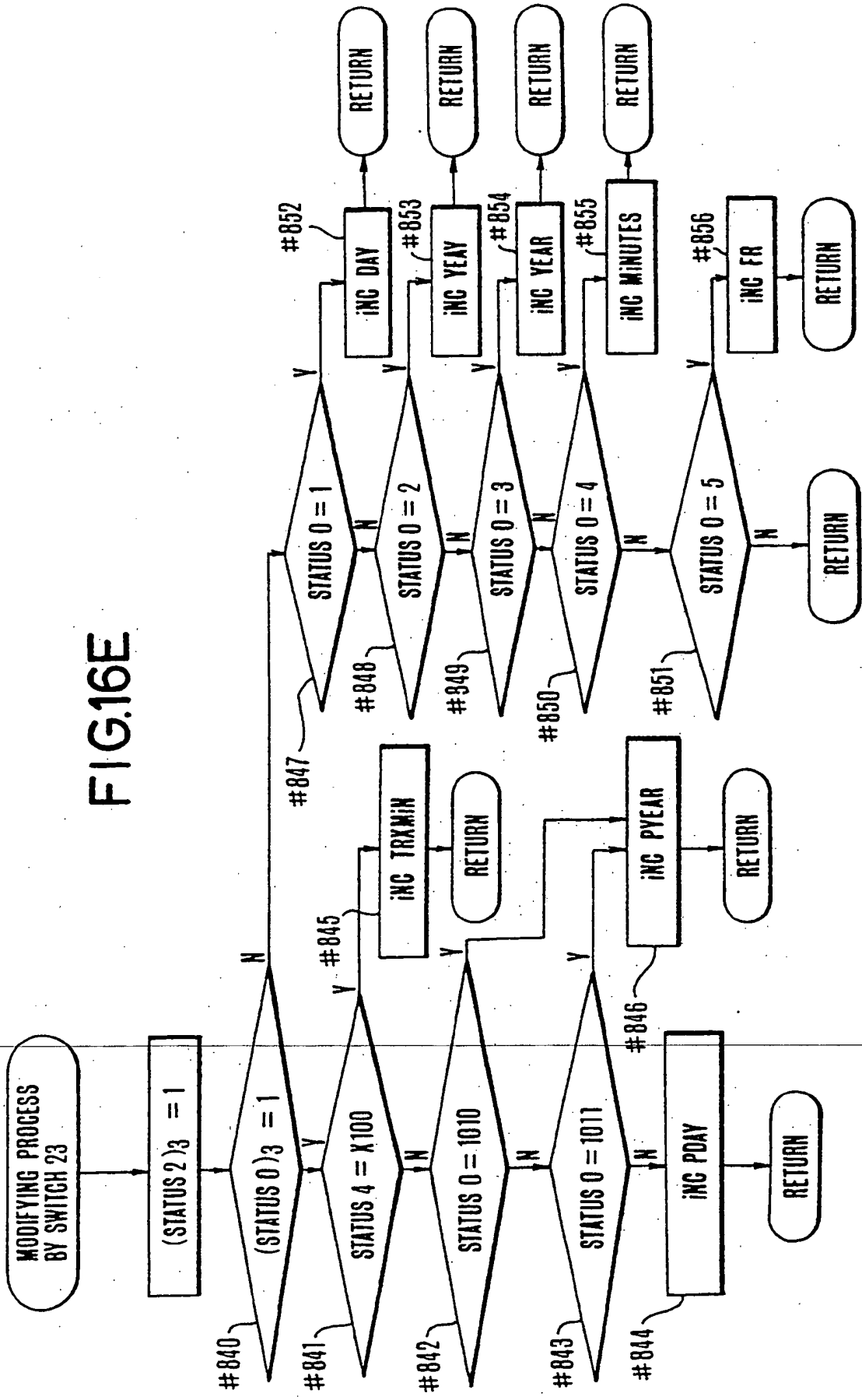
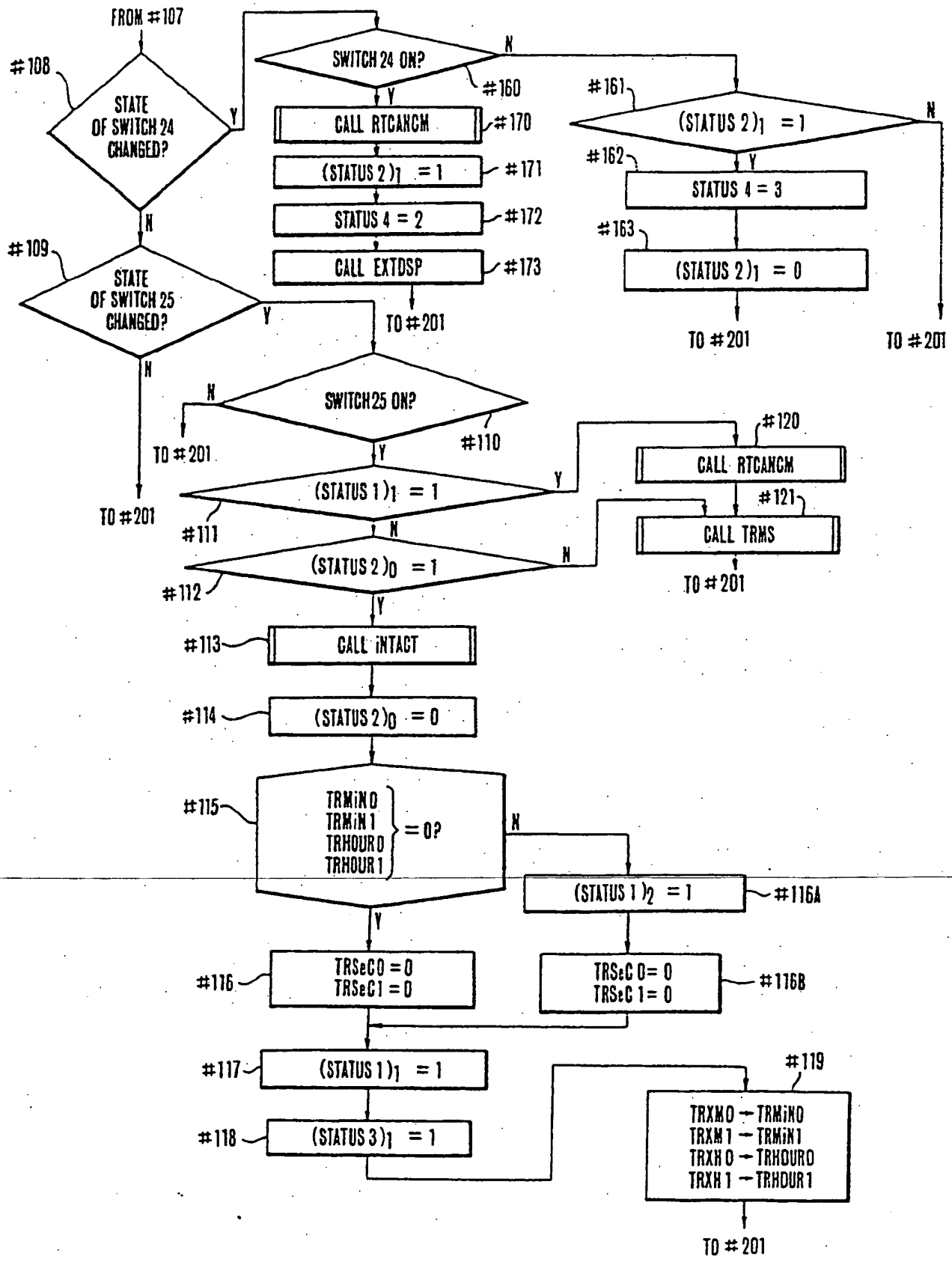

MODIFYING PROCESS BY SWITCH 23
(STATUS 2)3 = 1
(STATUS 0)3 = 1
STATUS 4 = X100
STATUS 0 = 1010
STATUS 0 = 1011
INC PDAY
RETURN
INC TRXMIN
INC PYEAR
STATUS 0 = 1
STATUS 0 = 2
STATUS 0 = 3
STATUS 0 = 4
STATUS 0 = 5
INC DAY
INC YEAY
INC YEAR
INC MINUTES
INC FR
#840
#841
#842
#843
#844
#845
#846
#847
#848
#849
#850
#851
#852
#853
#854
#855
#856
Y
N

FIG.16F


FROM #107
#108
STATE OF SWITCH 24 CHANGED?
Y
N
#109
STATE OF SWITCH 25 CHANGED?
Y
N
TO #201
SWITCH 24 ON?
N
Y
#160
CALL RTCANCM
#170
(STATUS 2)1 = 1
#171
STATUS 4 = 2
#172
CALL EXTDSP
#173
TO #201
#161
(STATUS 2)1 = 1
N
Y
#162
STATUS 4 = 3
#163
(STATUS 2)1 = 0
TO #201
TO #201
SWITCH 25 ON?
N
Y
#110
TO #201
(STATUS 1)1 = 1
Y
N
#111
TO #201
#120
CALL RTCANCM
#121
CALL TRMS
TO #201
(STATUS 2)0 = 1
N
Y
#112
#113
CALL INTACT
#114
(STATUS 2)0 = 0
#115
TRMIN0
TRMIN1
TRHOUR0
TRHOUR1
= 0?
N
Y
(STATUS 1)2 = 1
#116A
#116
TRSEC0 = 0
TRSEC1 = 0
TRSEC0 = 0
TRSEC1 = 0
#116B
#117
(STATUS 1)1 = 1
#118
(STATUS 3)1 = 1
#119
TRXM0 ← TRMIN0
TRXM1 ← TRMIN1
TRXH0 ← TRHOUR0
TRXH1 ← TRHOUR1
TO #201

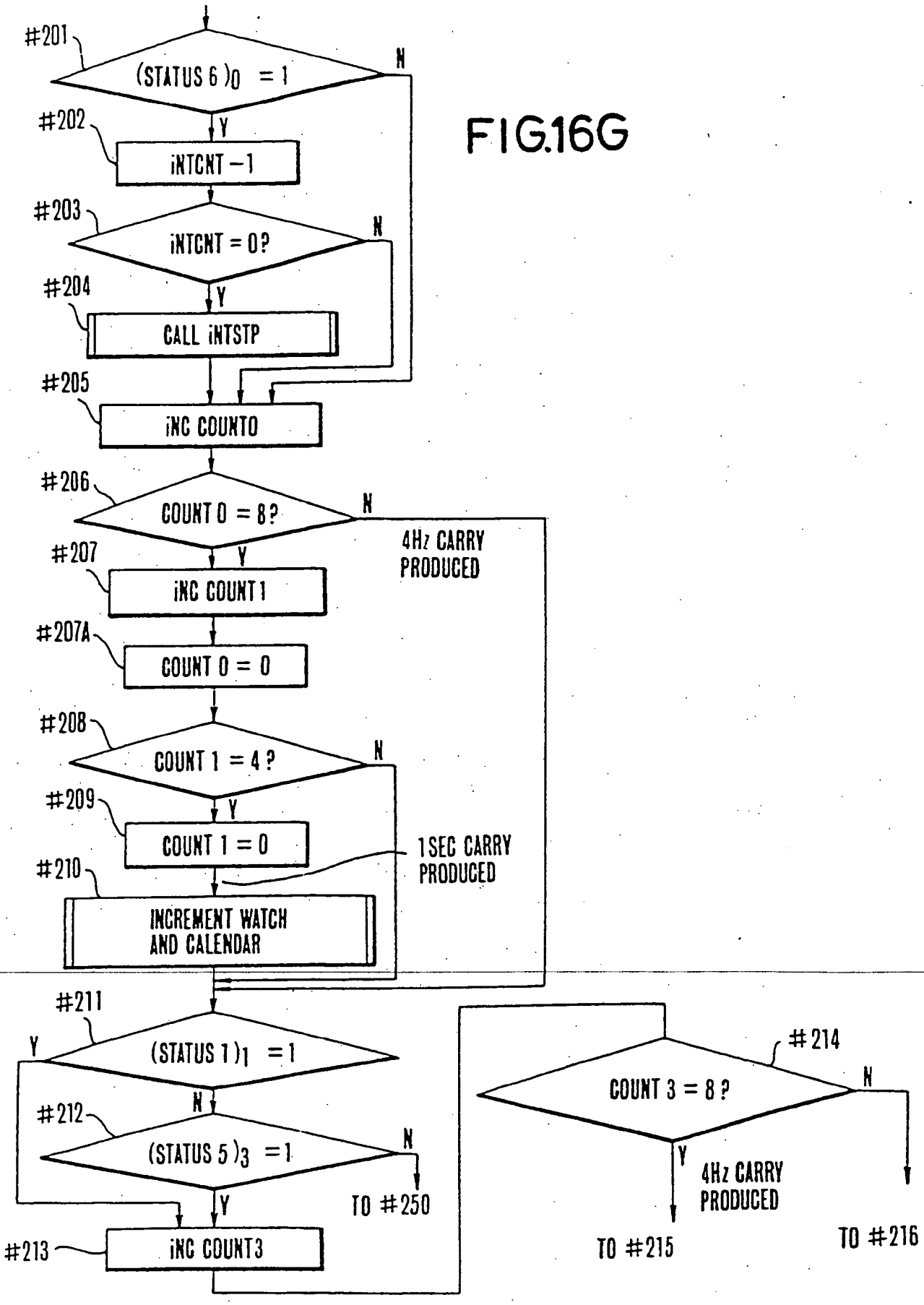

#201
(STATUS 6)0 = 1
N
Y
#202
iNTCNT −1
#203
iNTCNT = 0?
N
Y
#204
CALL iNTSTP
#205
iNC COUNTO
#206
COUNT 0 = 8?
N
4Hz CARRY PRODUCED
Y
#207
iNC COUNT1
#207A
COUNT 0 = 0
#208
COUNT 1 = 4 ?
N
Y
#209
COUNT 1 = 0
1SEC CARRY PRODUCED
#210
INCREMENT WATCH AND CALENDAR
#211
Y
(STATUS 1)1 = 1
N
#212
(STATUS 5)3 = 1
N
TO #250
Y
#213
iNC COUNT3
#214
COUNT 3 = 8 ?
N
Y
4Hz CARRY PRODUCED
TO #215
TO #216

FIG.16G

FIG.16H

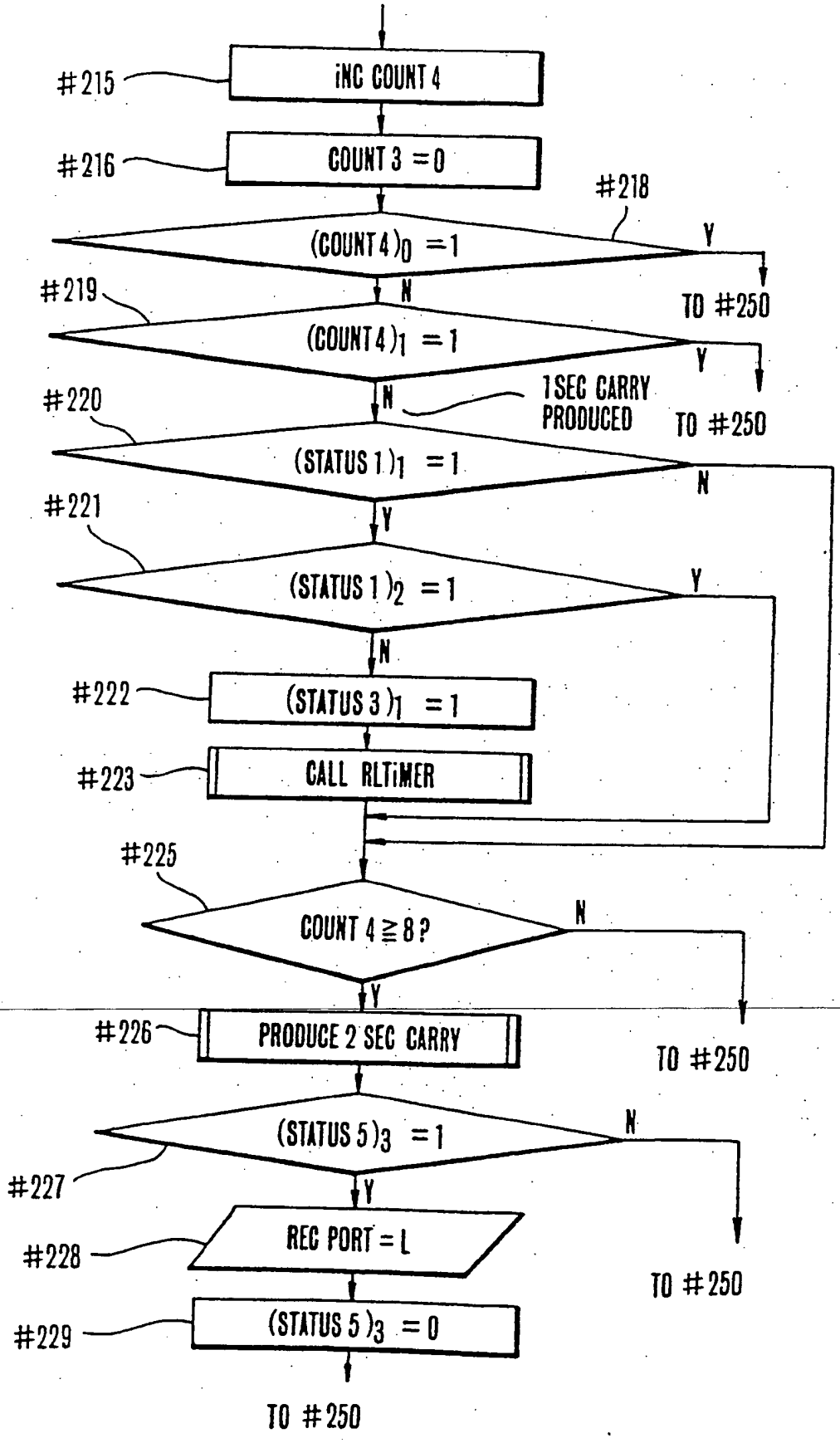

#215
INC COUNT 4
#216
COUNT 3 = 0
#218
(COUNT 4)0 = 1
Y
TO #250
N
#219
(COUNT 4)1 = 1
Y
TO #250
N
1SEC CARRY PRODUCED
#220
(STATUS 1)1 = 1
N
Y
#221
(STATUS 1)2 = 1
Y
N
#222
(STATUS 3)1 = 1
#223
CALL RLTIMER
#225
COUNT 4 ≧ 8 ?
N
Y
#226
PRODUCE 2 SEC CARRY
TO #250
(STATUS 5)3 = 1
N
#227
Y
#228
REC PORT = L
TO #250
#229
(STATUS 5)3 = 0
TO #250

FIG.16I

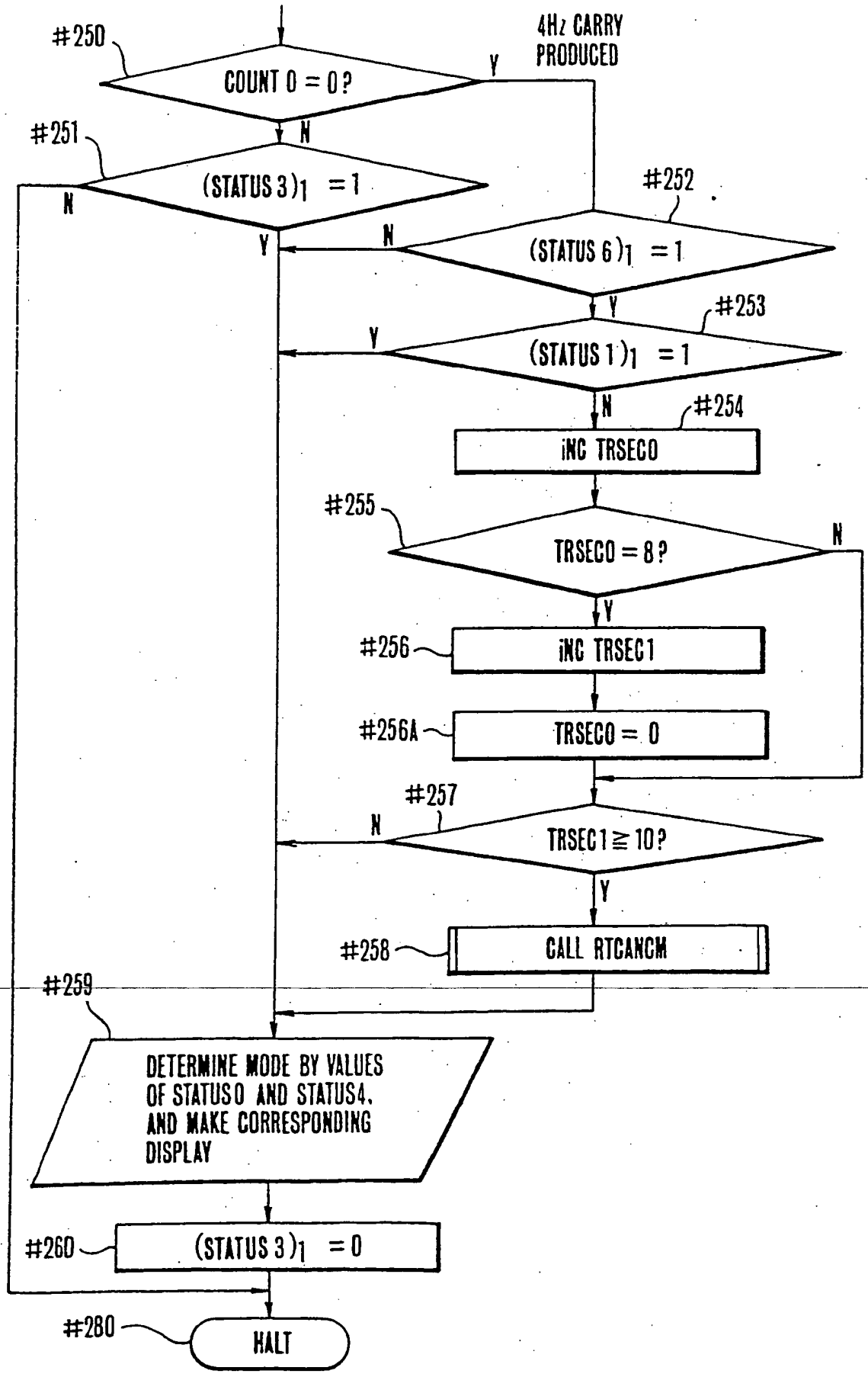

#250
COUNT 0 = 0?
Y
4Hz CARRY PRODUCED
N
#251
(STATUS 3)1 = 1
N
Y
#252
(STATUS 6)1 = 1
N
Y
#253
(STATUS 1)1 = 1
Y
N
#254
INC TRSEC0
#255
TRSEC0 = 8?
N
Y
#256
INC TRSEC1
#256A
TRSEC0 = 0
#257
TRSEC1 ≧ 10?
N
Y
#258
CALL RTCANCM
#259
DETERMINE MODE BY VALUES OF STATUS0 AND STATUS4, AND MAKE CORRESPONDING DISPLAY
#260
(STATUS 3)1 = 0
#280
HALT

FIG.16J

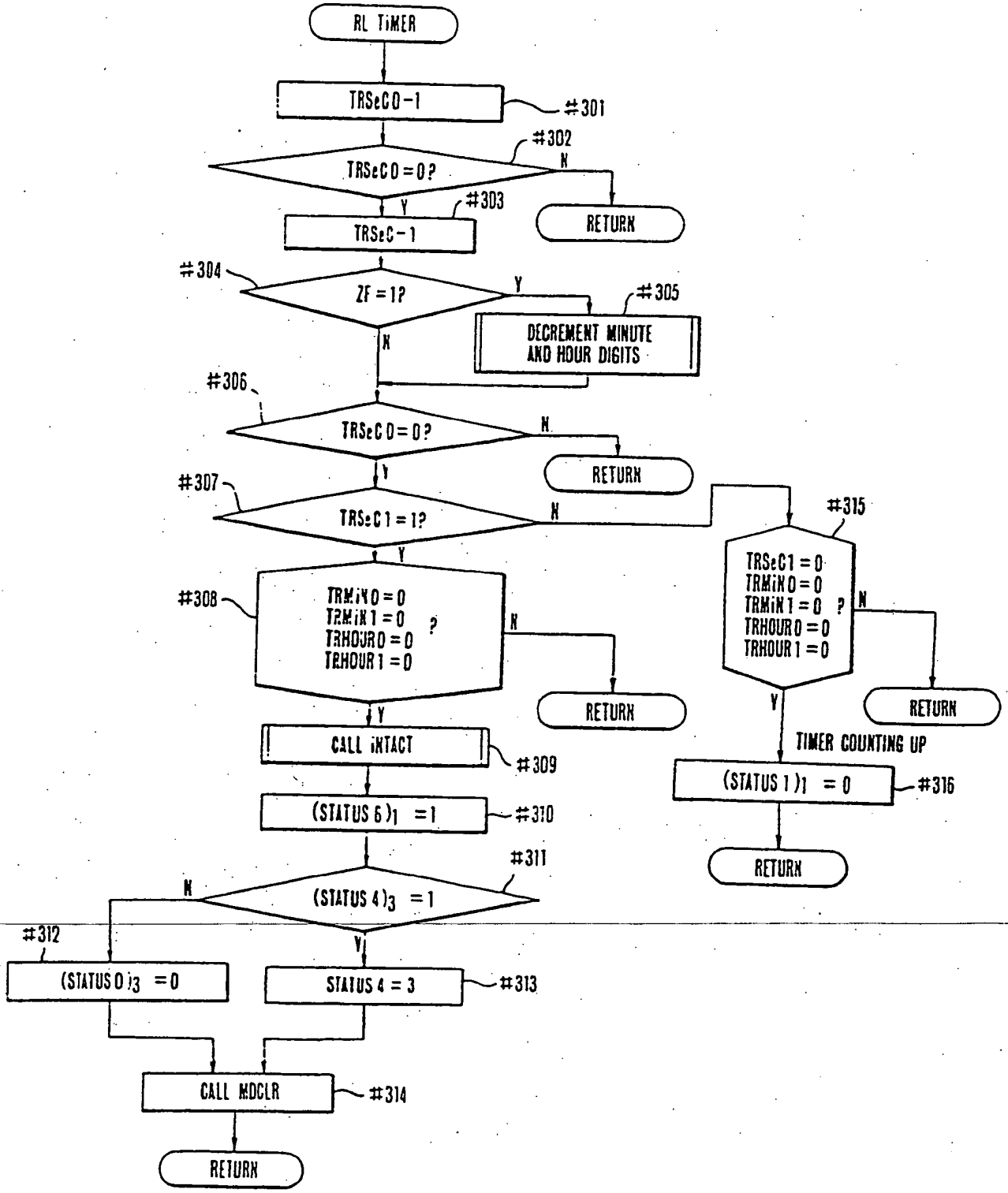

RL TIMER
TRSEC0-1
#301
#302
TRSEC0=0?
N
Y
#303
TRSEC-1
RETURN
#304
ZF=1?
Y
#305
DECREMENT MINUTE AND HOUR DIGITS
N
#306
TRSEC0=0?
N
RETURN
Y
#307
TRSEC1=1?
N
Y
#315
TRSEC1=0
TRMIN0=0
TRMIN1=0
TRHOUR0=0
TRHOUR1=0 ?
N
RETURN
Y
TIMER COUNTING UP
(STATUS 1)1 =0
#316
RETURN
#308
TRMIN0=0
TRMIN1=0
TRHOUR0=0
TRHOUR1=0 ?
N
RETURN
Y
CALL INTACT
#309
(STATUS 6)1 =1
#310
#311
N
(STATUS 4)3 =1
Y
#312
(STATUS 0)3 =0
STATUS 4=3
#313
CALL MDCLR
#314
RETURN

FIG.16K

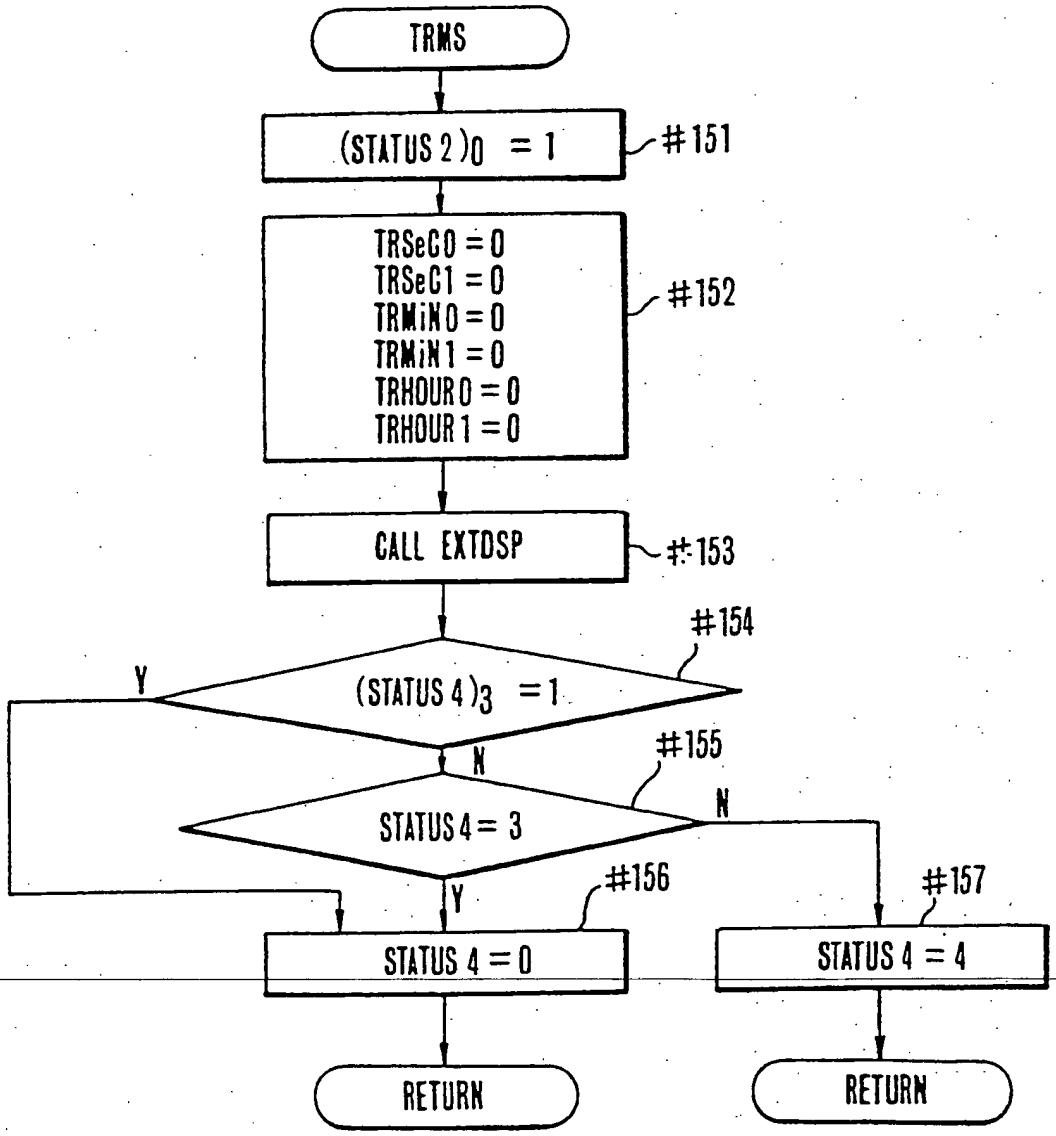
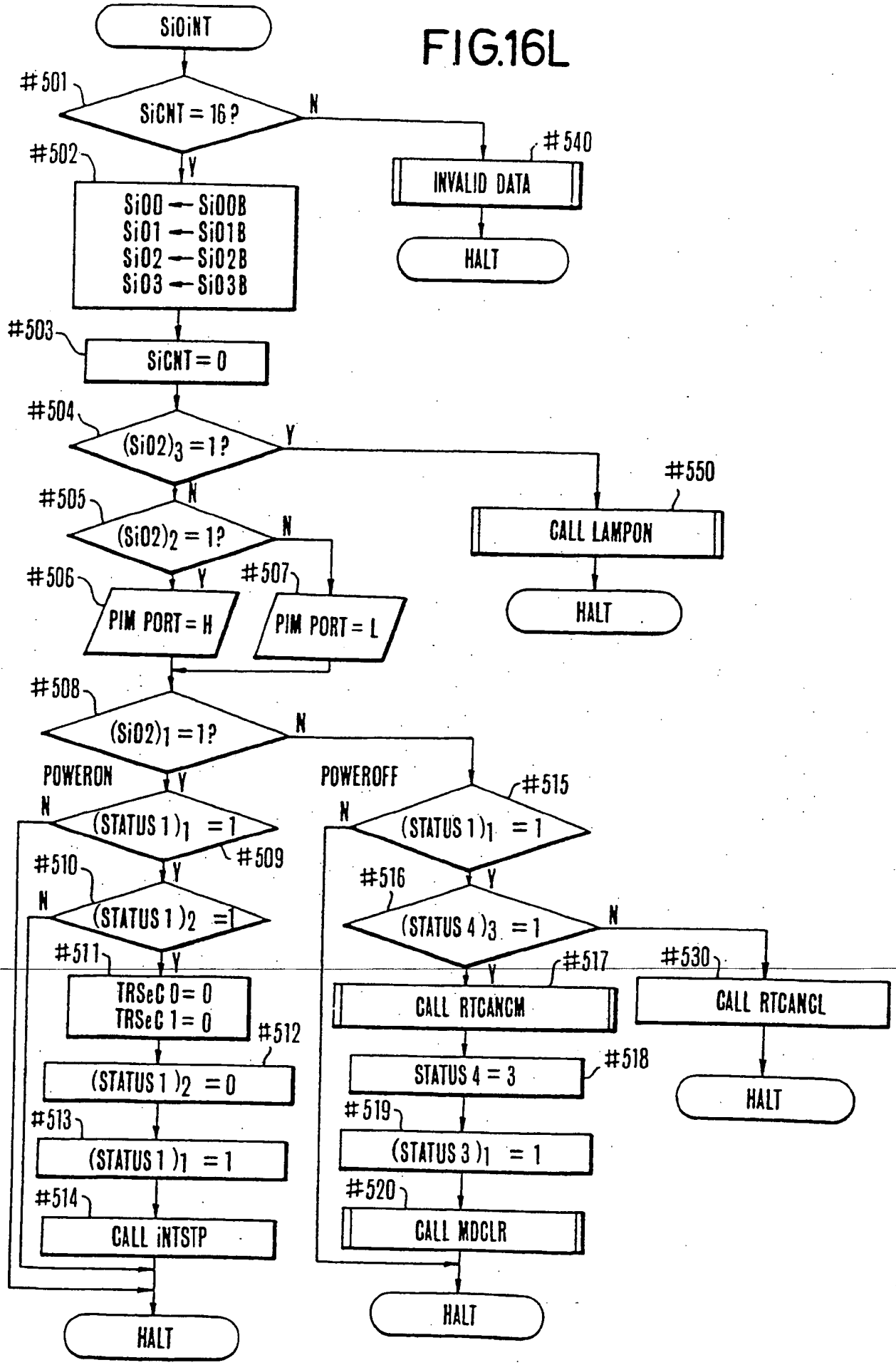

TRMS
(STATUS 2)0 = 1
#151
TRSeC0 = 0
TRSeC1 = 0
TRMiN0 = 0
TRMiN1 = 0
TRHOUR0 = 0
TRHOUR1 = 0
#152
CALL EXTDSP
#153
#154
(STATUS 4)3 = 1
Y
N
#155
STATUS 4 = 3
N
Y
#156
#157
STATUS 4 = 0
STATUS 4 = 4
RETURN
RETURN

FIG.16L


SiOiNT
#501
SiCNT = 16?
N
Y
#540
INVALID DATA
HALT
#502
Si00 ← Si00B
Si01 ← Si01B
Si02 ← Si02B
Si03 ← Si03B
#503
SiCNT = 0
#504
(Si02)3 = 1?
Y
N
#550
CALL LAMPON
HALT
#505
(Si02)2 = 1?
N
Y
#506
PIM PORT = H
#507
PIM PORT = L
#508
(Si02)1 = 1?
N
Y
POWERON
POWEROFF
N
(STATUS 1)1 = 1
#509
Y
#510
N
(STATUS 1)2 = 1
Y
#511
TRSeC 0 = 0
TRSeC 1 = 0
#512
(STATUS 1)2 = 0
#513
(STATUS 1)1 = 1
#514
CALL iNTSTP
HALT
#515
N
(STATUS 1)1 = 1
Y
#516
(STATUS 4)3 = 1
N
Y
#517
CALL RTCANCM
#530
CALL RTCANCL
#518
STATUS 4 = 3
HALT
#519
(STATUS 3)1 = 1
#520
CALL MDCLR
HALT

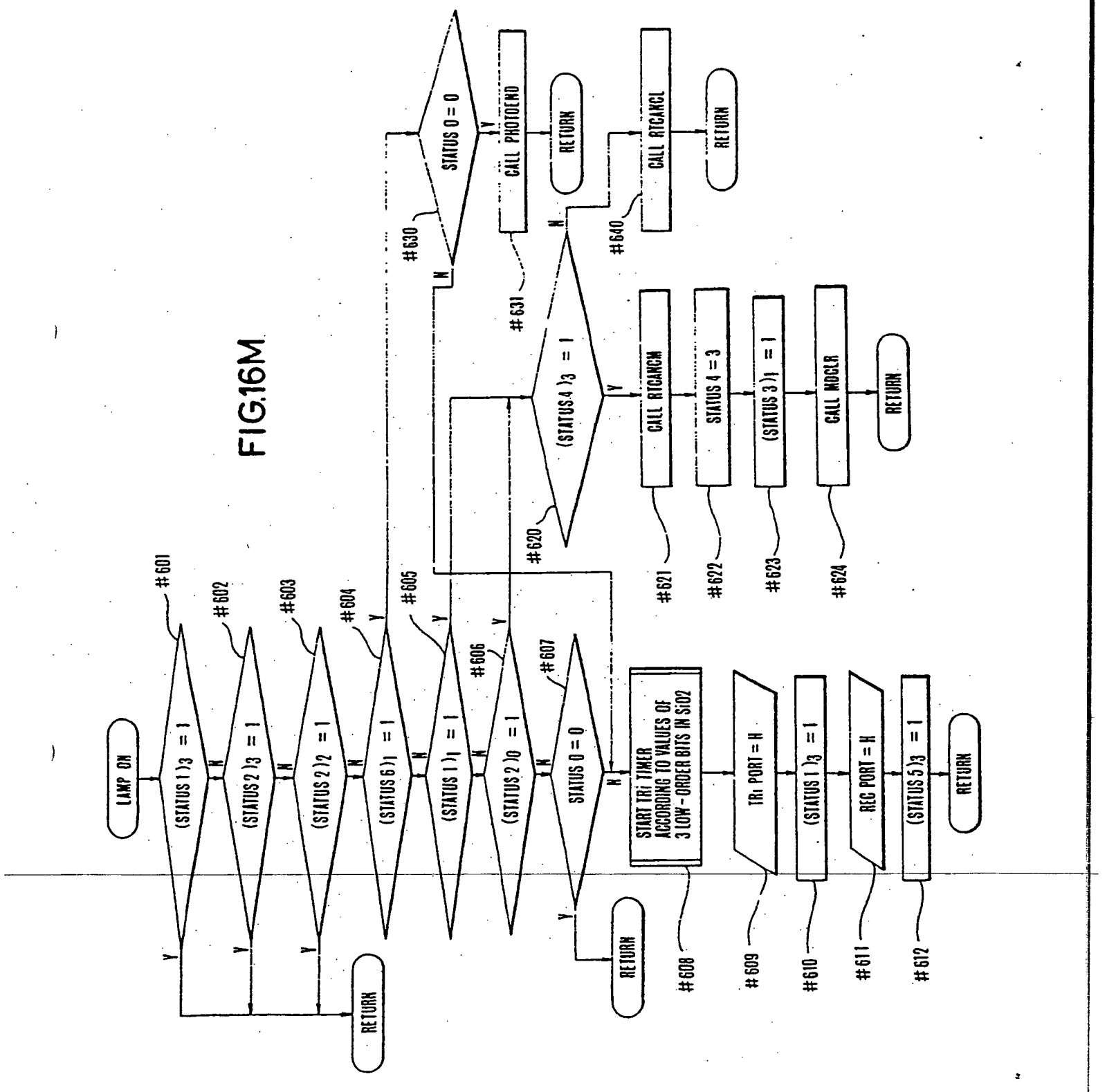

LAMP ON
(STATUS 1)3 = 1
(STATUS 2)3 = 1
(STATUS 2)2 = 1
(STATUS 6)1 = 1
(STATUS 1)1 = 1
(STATUS 2)0 = 1
STATUS 0 = 0
START TR1 TIMER ACCORDING TO VALUES OF 3 LOW-ORDER BITS IN SiO2
TR1 PORT = H
(STATUS 1)3 = 1
REG PORT = H
(STATUS 5)3 = 1
RETURN
#601
#602
#603
#604
#605
#606
#607
#608
#609
#610
#611
#612
STATUS 0 = 0
CALL PHOTOEND
#630
#631
(STATUS 4)3 = 1
CALL RTGANGL
#640
#620
CALL RTGANGM
STATUS 4 = 3
(STATUS 3)1 = 1
CALL MOGLR
#621
#622
#623
#624
Y
N

FIG.16M

FIG.16N

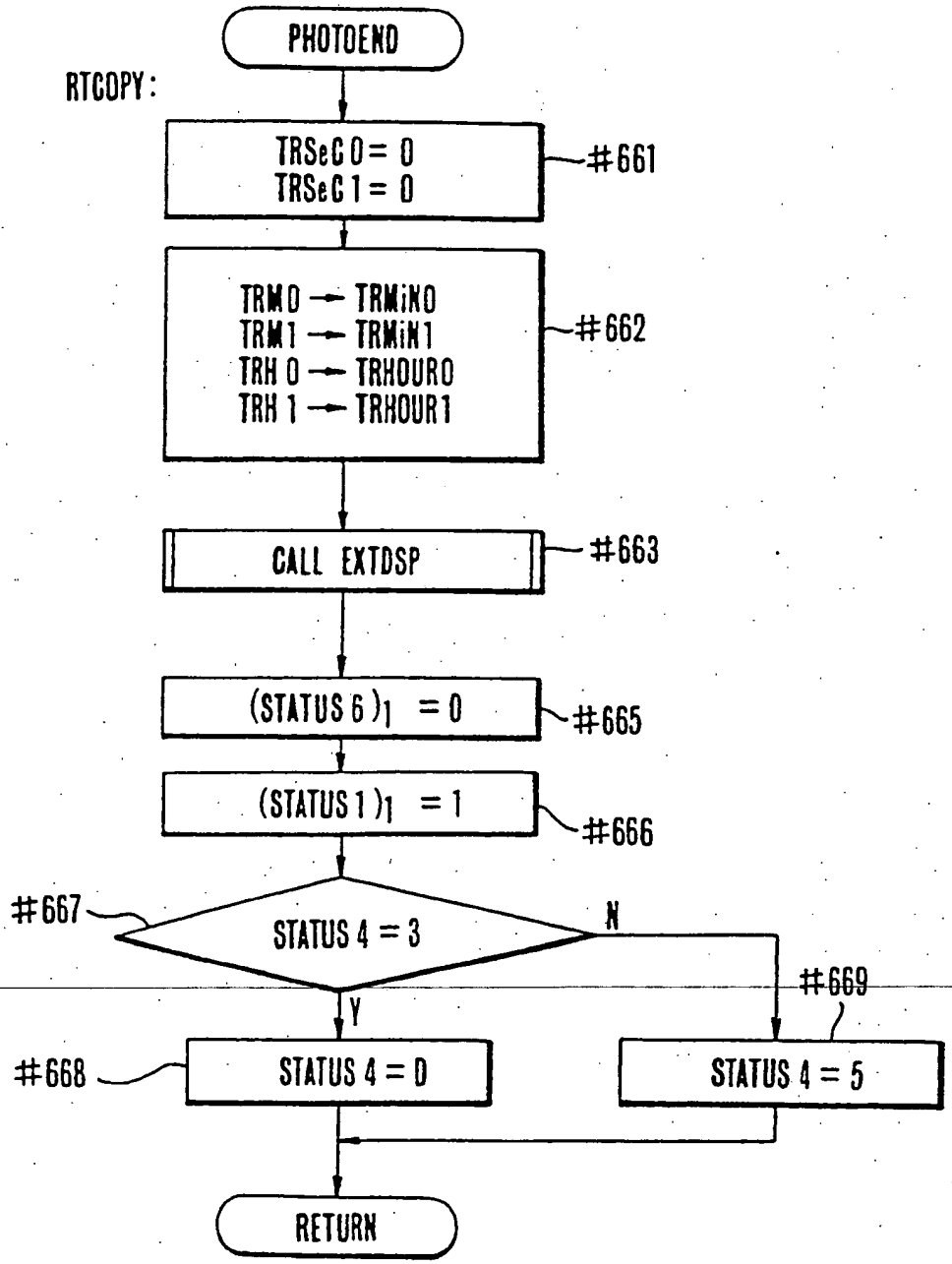

PHOTOEND
RTCOPY:
TRSeC 0 = 0
TRSeC 1 = 0
#661
TRM 0 → TRMiN0
TRM 1 → TRMiN1
TRH 0 → TRHOUR0
TRH 1 → TRHOUR1
#662
CALL EXTDSP
#663
(STATUS 6)1 = 0
#665
(STATUS 1)1 = 1
#666
#667
STATUS 4 = 3
N
Y
#669
#668
STATUS 4 = 0
STATUS 4 = 5
RETURN

FIG.16O

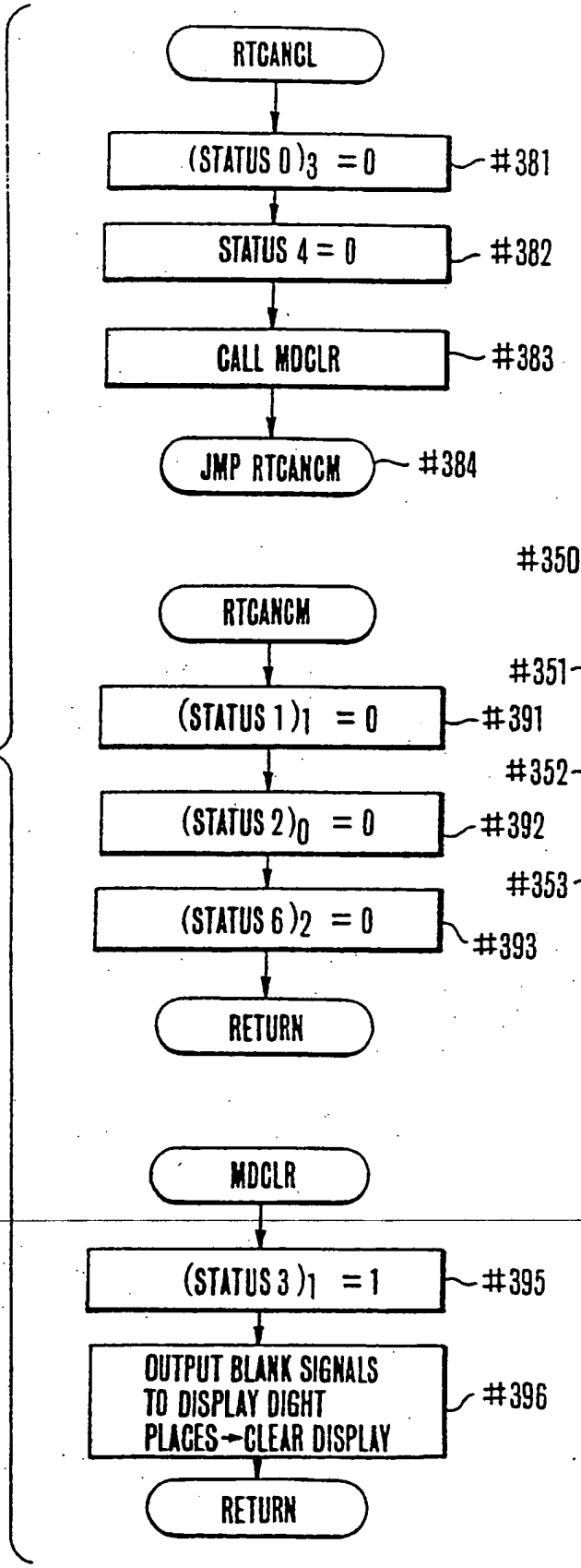


FIG.16P

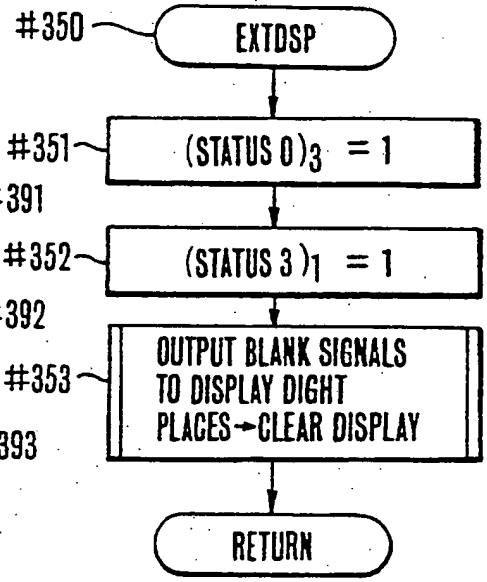


FIG.16Q

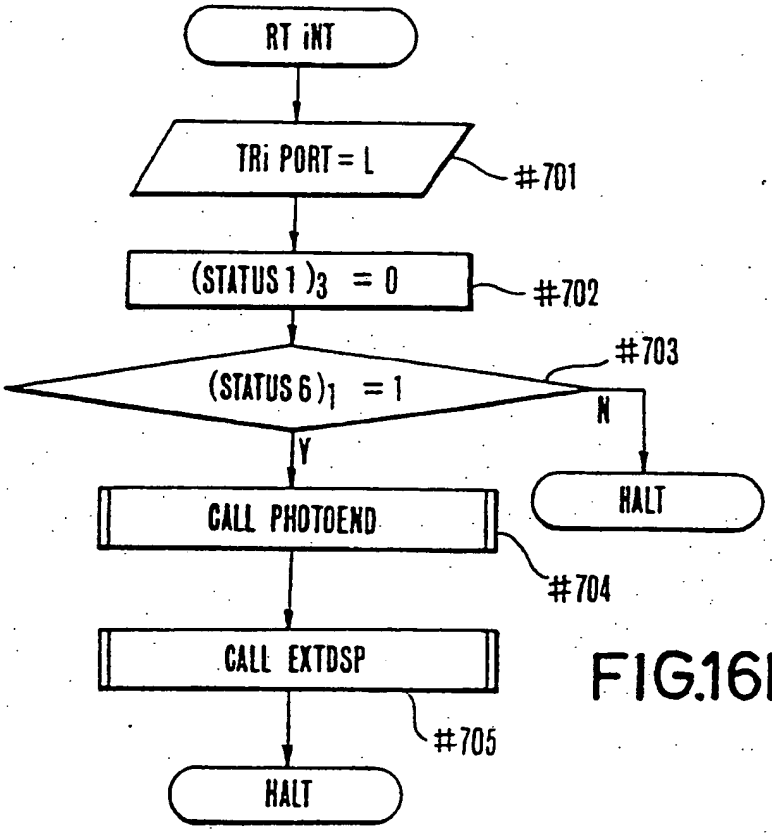


FIG.16R

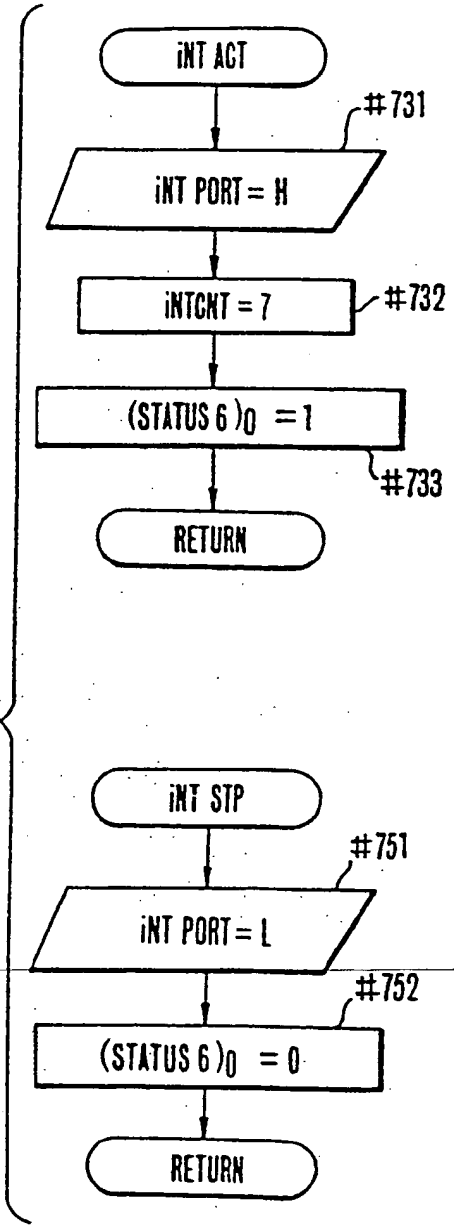
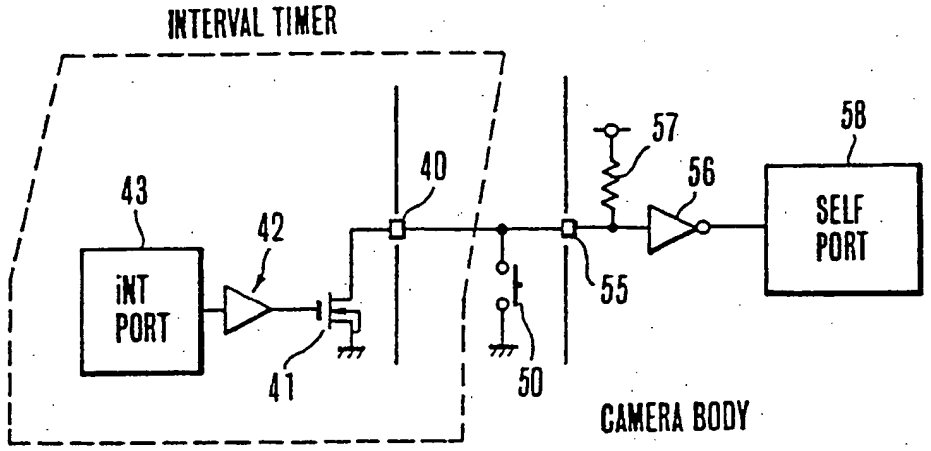


FIG.17


INTERVAL TIMER
43
42
40
57
58
56
SELF PORT
INT PORT
55
41
50
CAMERA BODY

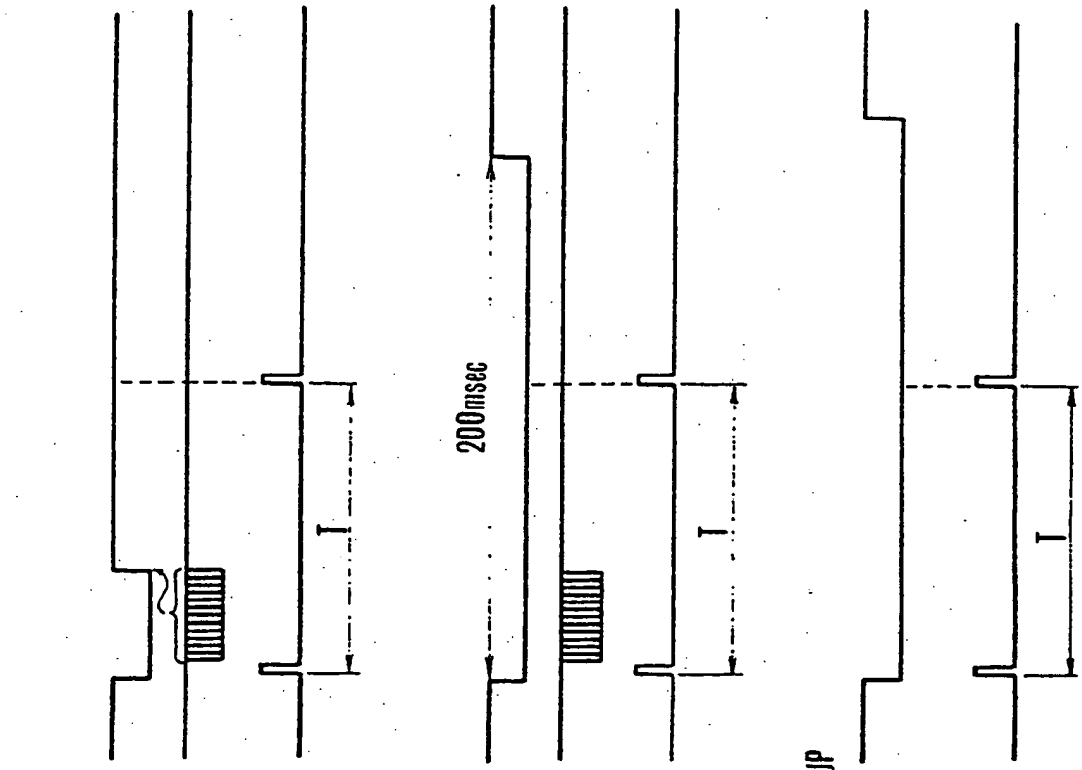


FIG.18A

FIG.18B

FIG.18C

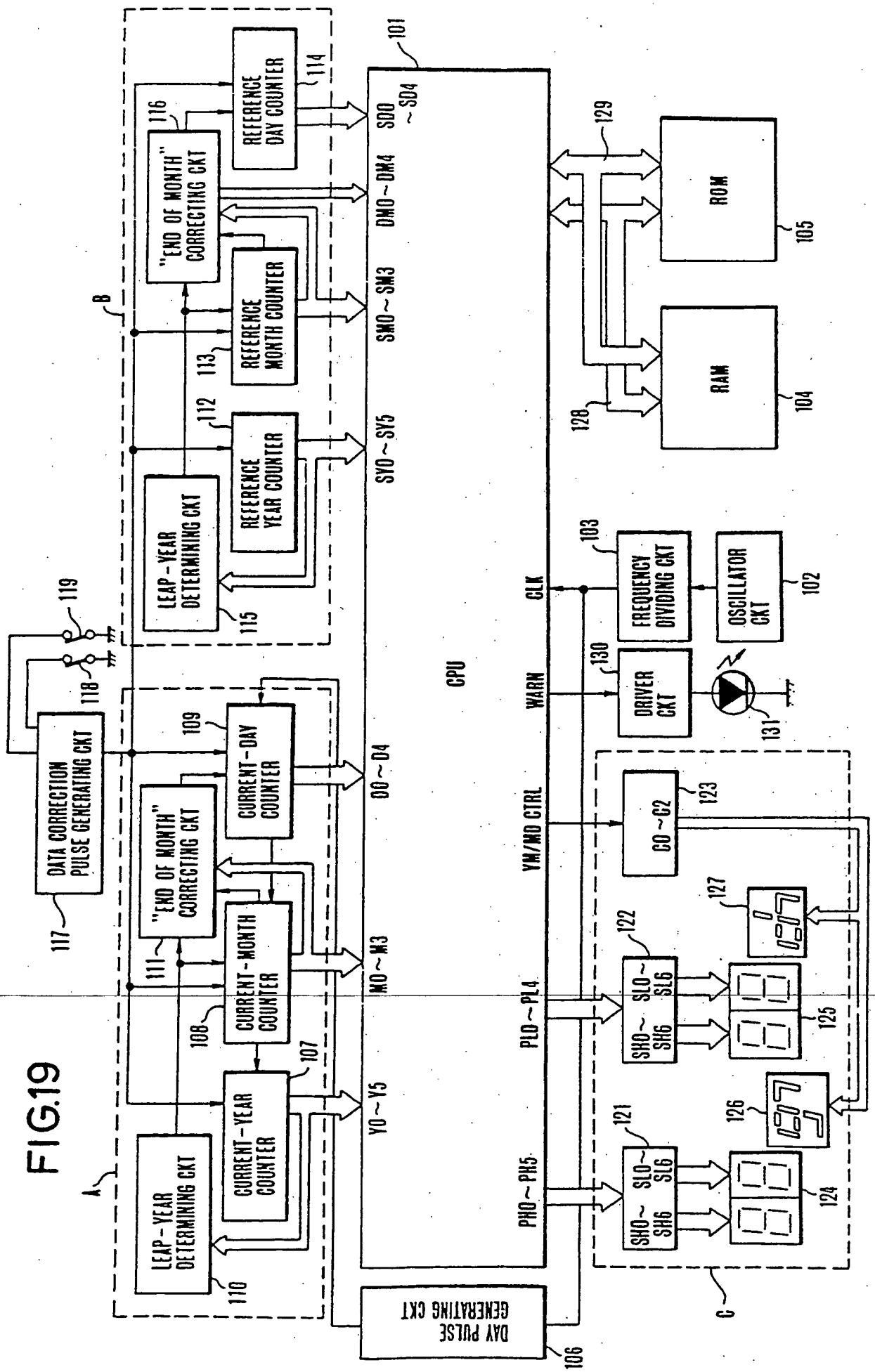

A
B
C
CPU
101
DATA CORRECTION PULSE GENERATING CKT
117
LEAP-YEAR DETERMINING CKT
110
CURRENT-YEAR COUNTER
107
CURRENT-MONTH COUNTER
108
"END OF MONTH" CORRECTING CKT
111
CURRENT-DAY COUNTER
109
LEAP-YEAR DETERMINING CKT
115
REFERENCE YEAR COUNTER
112
REFERENCE MONTH COUNTER
113
"END OF MONTH" CORRECTING CKT
116
REFERENCE DAY COUNTER
114
119
118
DAY PULSE GENERATING CKT
106
Y0~Y5
M0~M3
D0~D4
SY0~SY5
SM0~SM3
SD0~SD4
DM0~DM4
PH0~PH5
PL0~PL4
YM/MD CTRL
WARN
CLK
ROM
105
RAM
104
129
128
FREQUENCY DIVIDING CKT
103
OSCILLATOR CKT
102
DRIVER CKT
130
131
G0~G2
123
SH0~SH6
SL0~SL6
122
121
127
125
126
124

FIG.19

FIG.20

MEMORY ADDRESS LABEL	CONTENTS	PORT ADDRESS	INPUT/ OUTPUT
Y	CURRENT DATE YEAR DIGITS	Y0 ~ Y5	I
M	CURRENT DATE MONTH DIGITS	M0 ~ M3	I
D	CURRENT DATE DAY DIGITS	D0 ~ D4	I
SY	REFERENCE DATE YEAR DIGITS	SY0 ~ SY5	I
SM	REFERENCE DATE MONTH DIGITS	SM0 ~ SM3	I
SD	REFERENCE DATE DAY DIGITS	SD0 ~ SD4	I
PY	DIGITS OF PASSED YEARS	PY0 ~ PY5	—
PM	DIGITS OF PASSED MONTHS	PM0 ~ PM3	—
PD	DIGITS OF PASSED DAYS	PD0 ~ PD4	—
PH	HIGH-ORDER DIGITS OF TIME LAPSE DATA	PH0 ~ PH5	O
PL	LOW-ORDER DIGITS OF TIME LAPSE DATA	PL0 ~ PL4	O
DM	THE NUMBER OF DAYS IN THE REFERENCE MONTH	DM0 ~ PM4	I
YM/MD CTRL	YEAR-MONTH/MONTH-DAY DISPLAY SWITCHING	YM/MD. CTRL	O
WARN	WARNING DISPLAY CONTROL	WARN	O

FIG.21

DM OUTPUT	MONTHS CONCERNED
31	1. 3. 5. 7. 8. 10. 12.
30	4. 6. 9. 11
29	2 (IN LEAP-YEAR)
28	2 (IN NON-LEAP-YEAR)

FIG.22

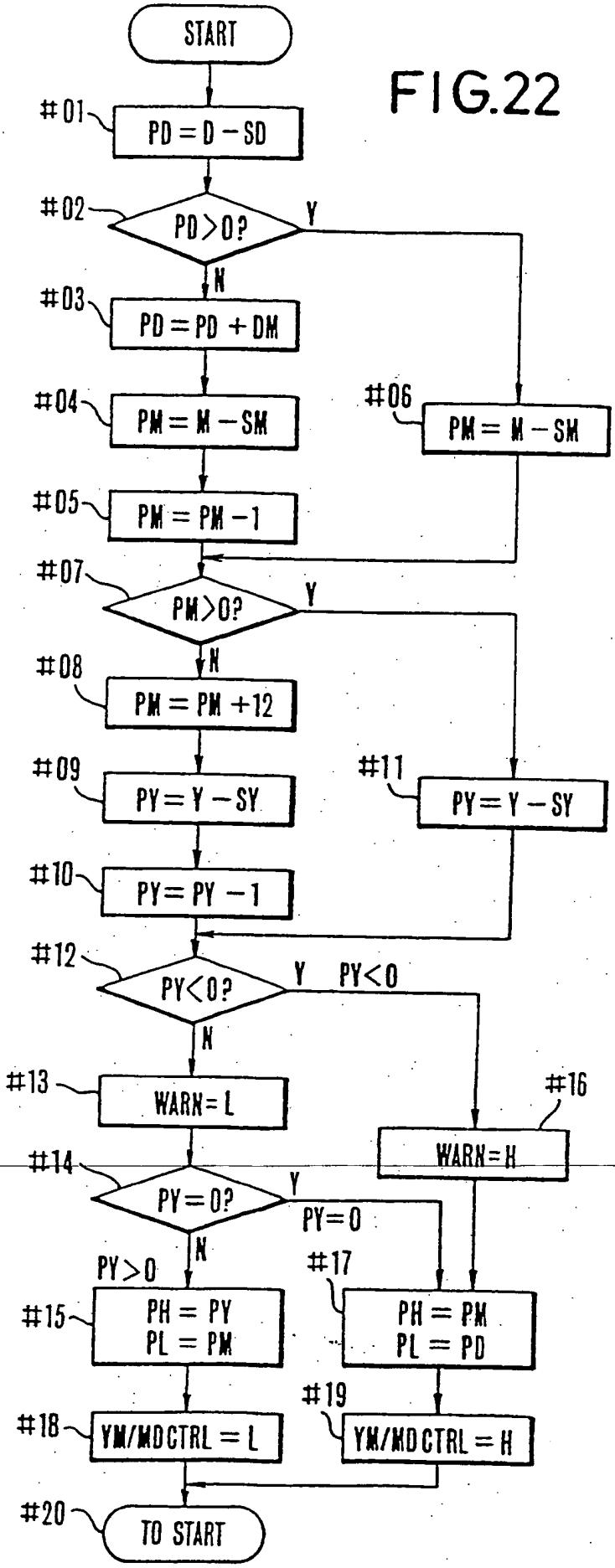
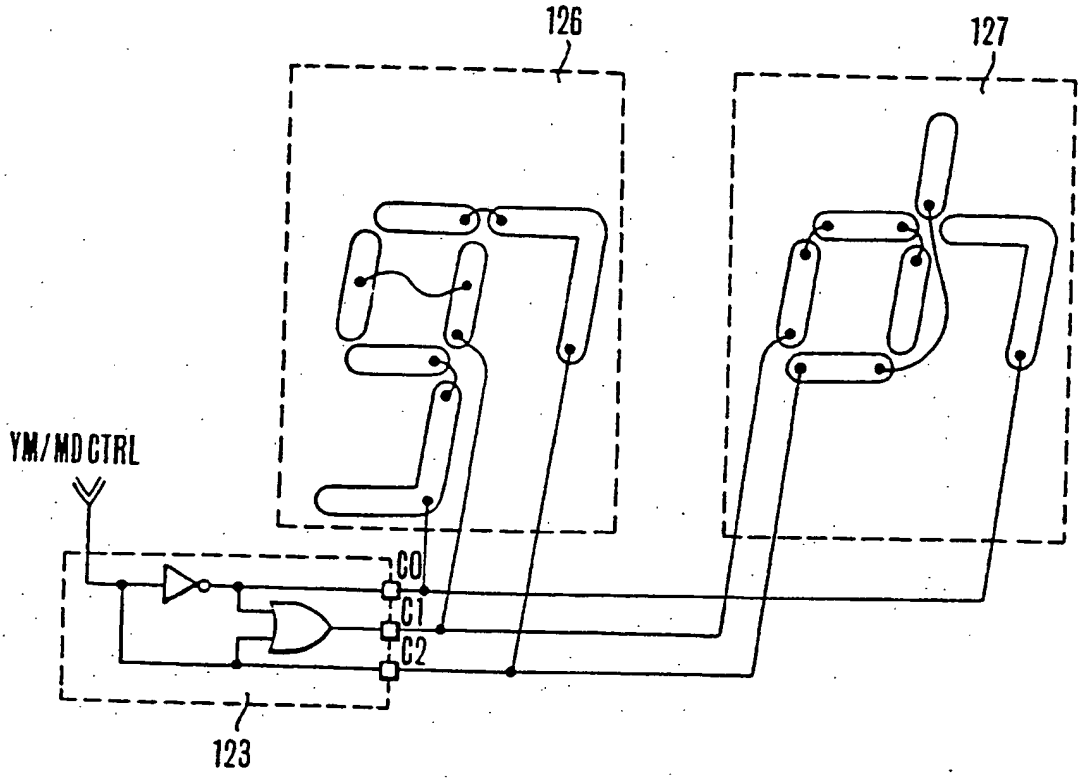

START
#01
PD = D − SD
#02
PD > 0?
Y
N
#03
PD = PD + DM
#04
PM = M − SM
#05
PM = PM − 1
#06
PM = M − SM
#07
PM > 0?
Y
N
#08
PM = PM + 12
#09
PY = Y − SY
#10
PY = PY − 1
#11
PY = Y − SY
#12
PY < 0?
Y
PY < 0
N
#13
WARN = L
#14
PY = 0?
Y
PY = 0
N
PY > 0
#15
PH = PY
PL = PM
#16
WARN = H
#17
PH = PM
PL = PD
#18
YM/MDCTRL = L
#19
YM/MDCTRL = H
#20
TO START

FIG.23



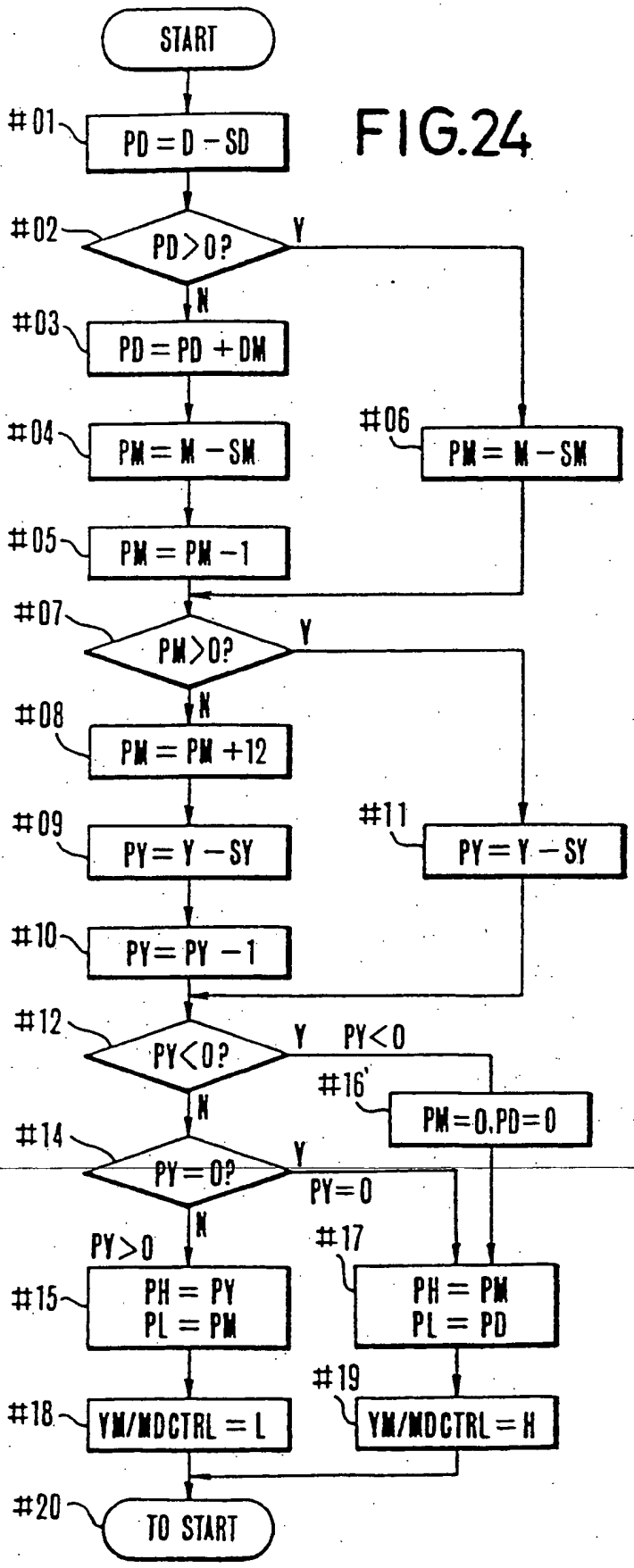

START
#01
PD = D − SD
#02
PD > 0?
Y
N
#03
PD = PD + DM
#04
PM = M − SM
#05
PM = PM − 1
#06
PM = M − SM
#07
PM > 0?
Y
N
#08
PM = PM + 12
#09
PY = Y − SY
#10
PY = PY − 1
#11
PY = Y − SY
#12
PY < 0?
Y
PY < 0
N
#16'
PM = 0, PD = 0
#14
PY = 0?
Y
PY = 0
N
PY > 0
#15
PH = PY
PL = PM
#17
PH = PM
PL = PD
#18
YM/MDCTRL = L
#19
YM/MDCTRL = H
#20
TO START

FIG.24

2242753

CAMERA AND PHOTOGRAPHIC DEVICE

The present invention relates to a camera arranged for performing time-lapse photography and to an interval-photography device for a camera.

There have been many proposals for cameras suitable for performing time-lapse photography, referred to herein as "interval shootable cameras", in which pictures are taken at fixed time intervals. However, these cameras suffer from one or more of the following inconveniences.

First, a conventional interval shootable camera comprises an interval shooting timer the operation of which is not designed to stop should the shutter release on the camera body be operated whilst the timer is operating.

Such a timer would be sufficient if the photographer desired to continue time-lapse photography after having released the shutter. If he did not desire to do so and failed to stop the timer, however, the interval timer would continue to operate for photography, contrary to his intention.

Second, a conventional timer for a camera is so designed that it will not start operating if it is reset - that is, set to zero during a time interval. Consequently, there would be no photography operation if the photographer intended to take pictures by using

the interval timer but failed to start the interval timer. Besides, a camera having an interval timer that can be set only in minutes could not take pictures at intervals of less than one minute by using the interval timer.

Third, a conventional interval timer for several cameras is designed so as to transmit release signals to the individual cameras each time the preset time has been counted. For compact cameras equipped with electronic flash devices which can flash automatically in the dark, the interval timer would have to latch the release signals until the cameras have completed charging of the flash devices, before releasing the shutters in the case of photography in dark environments. Such timers and cameras would encounter an inconvenience in that the transfer of the release signals between the cameras is complicated.

Fourth, the interval timer in the interval shooting system of many conventional cameras is designed so that the interval time may only be set in hours, minutes and seconds. However, sometimes a situation arises where an interval time of only seconds is required for operating the interval shooting system. In addition, the switching and other operations are complicated for time setting.

Fifth, an interval for conventional cameras with backcover data imprinting device is designed so that

the interval time can be set and started only while the main switch on the camera body is set OFF. However, the camera will not take a photograph with its main switch set OFF.

If the photographer fails to turn on the main switch of his camera but starts the interval timer, he would find and regret that his camera had taken no picture.

Sixth, if one and the same display unit is used both as a data monitor unit and an interval timer setting display unit in a camera with a data imprinting device, the display would be switched to the data imprinting information when the interval timer is started to count the set interval time, while operation of the timer is displayed, for example, by a small flashing dot at a corner of the display screen. However, the timer operation cannot easily be viewed at a glance, by way of the small flashing dot.

A principal object of the present invention is to minimise at least one of the inconveniences as discussed above of the known camera arrangements for performing time-lapse photography.

According to the present invention, therefore, a camera arranged for performing time-lapse photography comprises:

timer means for time-lapse photography; and

prohibition means for prohibiting said timer means from

operating when a camera main switch on the camera body is in the off state.

It will be appreciated that in this invention, should the principal camera switching means be set OFF, the interval shooting means will not be started, with the display unit providing no count-down indication, which informs the photographer that the camera switching means is OFF. Thus, such a failure where the camera takes no photograph owing to the photographer's error in camera operation can be prevented.

This invention extends to an interval photography device for a camera arranged to have the functionality described above.

This invention will now further be described, but by way of illustration only, referring to the accompanying drawings, which show embodiments of the invention and details thereof. In the drawings:

Fig. 1 is a back view of a camera according to the present invention.

Fig. 2 is a cross-sectional view showing the main part of the dating mechanism on the back side of the camera.

Fig. 3 is a block diagram showing the electronic control circuit of the camera.

Fig. 4 is a layout of monitor LCD segments.

Figs. 5 to 14 are views illustrating the displays of monitor LCDs respectively.

Figs. 15A to 15D are flow charts illustrating the control software.

Figs. 16A to 16R are detailed flow charts corresponding to the flow charts shown in Figs. 15A to 15D.

Fig. 17 is a circuit diagram showing the interconnection between the interval timer and the camera body.

Figs. 18A to 18C are timing charts showing the timer operation.

Fig. 19 is a block diagram showing the circuit configuration of a time lapse calculator which may be used in an embodiment of the present invention.

Fig. 20 is a table listing the inputs and outputs of the I/O ports on the central processing unit (CPU) in the calculator as shown in Fig. 19.

Fig. 21 is a table listing the outputs from

the "end of month" correcting circuit 116 in the calculator as shown in Fig. 19.

Fig. 22 is a flow chart showing a program run in the CPU 101 as shown in Fig. 19.

Fig. 23 is a schematical view showing the configuration of a decoder 123 and unit display sections 126 and 127 contained in a block C as shown in Fig. 19.

Fig. 24 is a flow chart showing a partial modification of the flow chart as shown in Fig. 22.

A preferred embodiment of system according to the present invention will be described below in reference to Figs. 1 to 18C.

Fig. 3 is a block diagram showing the circuit configuration of a data imprinting device with interval timer facility.

In this figure, the part on the right side relative to the disconnecting line shows a control circuit contained in the camera body 46. 1 is a central processing unit (hereinafter referred to as CPU) in a microcomputer which provides the sequence control for the operation of the entire system according to the present invention as well as the change and time counting of a watch and calendar and the control of timers. 3 is a PUC circuit which delivers a powerup clear signal when a battery 2 of the camera is switched on. When this signal enters the RESET (RE) terminal of the CPU

1, the CPU 1 is reset. 4 is an oscillator which generates reference clock pulses (CLKs). When this signal enters the input terminal CLK in the CPU 1, all the operations of circuits in this system are synchronized. 5 is a frequency dividing circuit which divides the frequency of the CLK pulse into 32Hz in this embodiment, which enters the 32HziNT terminal of the CPu 1. 6 is a TRi timer which counts the lighting time of a data imprinting lamp 14. When the count reaches zero (0), the TRi timer 6 enters an interrupt signal TRiNT into the CPU 1. 7 is a ROM which stores the contents of a program. 8 is a RAM which reads out and writes in data.

10 is a monitor LCD. 11 is a data imprinting LCD. The two LCDs are mounted inside the back cover 45 of the camera, and display the data imprinting information, the operation of the interval timer, the data imprinting recognition (REC) mark 37, the photographing information (PIM) mark 36, etc. with the signals from the segment (SEG) terminals, common (COM) terminal, REC terminal and PIM terminal on an LCD driver 9.

A data imprinting circuit is connected to the base of a transistor 12 and the emitter of a transistor 13 through a buffer 15 connected to the TRi terminal of an I/O port 17, the two transistors 12 and 13 being used to drive the data imprinting lamp 14. The transistor 12 comprises a collector connected to the positive pole of a power battery and an emitter connected too one of

the terminals on the data imprinting lamp 14. The transistor 13 comprises a base connected to the output terminal of a constant-voltage circuit 16 to drive the lamp 14 with the constant voltage, and an emitter grounded together with the other terminal of the lamp 14.

An N-channel MOS transistor 18 is connected to the iNT terminal of the I/O port 17. This MOS transistor 18, turned on, can apply a low level to the SELF terminal of a camera sequence control circuit 52 as a self-timer switch 50 on the camera body 46 is set to ON. When the MOS transistor 18 and the self-timer switch 50 are set to OFF, the SELF terminal is pulled up by a pull-up resistor 51 to a high level.

19 is a serial interface circuit which receives information from the camera body 46. The chip select (CS) terminal, serial clock (SCK) terminal and serial data input (SDI) terminal of the serial interface circuit 19 are connected separately to the camera sequence control circuit 52. The serial interface circuit 19 is also connected to the SiOiNT terminal of the CPU 1 to deliver an interrrupt signal to the CPU 1 with a serial code entered in the circuit 19.

On the I/O port 17, terminals S0, S1, S2, S3, S4 and S5 are connected to a data imprinting mode selector switch 20, imprinting data and interval timer time modifying switches 21, 22 and 23, a time lapse imprinting mode selector switch 24 and an interval timer mode switch 25 respectively and also connected to pull-up resistors

26, 27, 28, 29, 30 and 31 respectively to be pulled up.

The CPU 1, the TRi timer 6, the ROM 7, the RAM 8, the I/O port 17 and the serial interface circuit 19 are connected with each other through an address bus 32 which transfers program addresses, a data bus 33 which transfers and receives data, and a control bus 34 which controls the timing of the address and data transfer.

53 is the main switch of the camera body, which is pulled up by a pull-up resistor 54 when it is in OFF, and connected to the main switch (MSW) terminal on the camera sequence control circuit 52.

Fig. 1 is a back view of the camera, and Fig. 2 is the cross-sectional view showing the main part of the camera back portion.

In Figs. 1 and 2, 45 is the back cover of the camera, which is placed and designed so that the monitor LCD 10 can be viewed on the back side of the camera and that the switches 20 to 25 can be operated there. This monitor LCD 10 comprises a film counter display section 35, a camera body operation indicating mark 36, a data imprinting recognition mark 37, and display section 38 to recognize the imprinting data selected by the switches 20 to 25.

On the inside of the back cover 45 is placed the data imprinting LCD 11 connected in series to the monitor LCD 10. The data displayed on the data imprinting LCD 11 are to be imprinted by the data imprinting lamp 14 on the surface of a film F serving as photosensitive

means placed in the camera body 46.

The operation of this embodiment thus configured and constructed will be described below.

At first, the display of the imprinting data recognition display section 38 as well as the display in the interval timer mode and the display in the time lapse imprinting mode will be described.

Concerning the display of the imprinting data recognition display section 38, this display section 38 displays selectively the calendar data in the forms of "year/month/day", "month/day/year", "day/month/year" and "day/hour/minute" as well as the "film exposed-frame number information imprinting mode" (hereinafter referred to as FC mode) and "imprinting OFF mode" in this order each time when a data imprinting mode selector switch 20 is turned on. This display section 38 has a segment layout to display any of the abbreviated month names in English, and by operating the switch 20, permits to display any English month name (Fig. 5) as well as any month name in numerical form (Fig. 6) selectively. If any calendar information such as "year/month/day", "month/day/year", "day/month/year" or "day/hour/minute" is displayed on the display section 38, each display may be incremented by operating the imprinting data modifying switches 21, 22 and 23.

Concerning the interval timer mode, when the interval timer mode switch 25 is turned on, the display section 38 is switched from the data imprinting mode

into the interval timer mode and displays in hour and minute the time Ti which passes from the pressing of the release button to the generation of a release signal (Fig. 9). Such display may be modified by means of the modifying switches 22 and 23.

When the interval timer mode switch 25 is turned on again, the display section 38 starts the operation as the countdown timer by adding the data in second, as shown in Fig. 10 if the main switch 53 on the camera body 46 is set in ON. If the main switch 53 on the camera body 46 is in OFF, however, the display section 38 is switched into the display format which had been provided before it was switched into the interval timer mode, and does not provide the countdown information any more. Operating as the countdown timer, the display section 38 then recovers the display format which had been provided before it was switched into the interval timer mode (for example, Figs. 5 to 7), 10 seconds before the release is operated, and the CPU 1 transmits a self-timer startup signal to the camera body 46.

When the signal indicating that the release is operated enters the CPU 1 through the serial interface circuit 19, the display section 38 starts to operate again as the countdown timer on countdown-displaying the time Ti in second. If the release end signal does not enter the CPU 1 within the predetermined time after the self-timer started up, the interval timer mode is cancelled, and the display section 38 recovers the display

format which had been provided before it was switched into the interval timer mode, and does not provide the countdown display any more. If any release signal enters the circuit of this display section 38 from the camera body during the counting-down by the interval timer, or if the data imprinting mode selector switch 20 is turned on during the countdown operation, the countdown operation is stopped and the display section 38 recovers the display format which had been provided before it was switched into the interval timer mode.

Concerning the time lapse imprinting mode (hereinafter referred to as "PA mode"), the display section 38 is switched into the time lapse display mode despite of providing the previous display format in data imprinting mode, when the time lapse imprinting switch 24 is turned on.

When the switch 24 is in ON, the date "year/month/day" from which the lapse of time is counted is displayed (Fig. 11). While this switch 24 is being pressed down, the starting date (year/month/day) may be modified by means of the modifying switches 21 to 23.

The date "year/moth/day"is displayed in the format which had been provided before the display section 38 is switched into PA mode, if it is possible. If it is impossible, for example, if the display has been in the format "day/hour/minute" in imprinting mode, or if the display section 38 has been in "FC mode" or

"imprinting OFF mode", the date "year/month/day" is displayed in numerical format as shown in Fig. 11.

Next, when the switch 24 is turned off, the lapse of time (the current date to the count starting date) ΔT is displayed, and it is imprinted when the date signal from the camera body 46 enters the circuit of the display section 38.

It is understood that the lapse of time ΔT is updated as the current date is updated.

The display format on the display section 38 is "year/month" (in the display form of "XyXm" wherein X denotes a numeral, y denotes the year and m denotes the month.) for $\Delta T > 12$ months (Fig. 12), "month/day" (in the display form of "XmXd" wherein d denotes the day.) for $\Delta T \leq 12$ months (Fig. 13), and "0 month/0 day" (in the form of "OmOd" for $\Delta T \leq 0$ (Fig. 14), as shown in Figs. 12 to 14.

Incidentally, the above small letters "y" and "m" are displayed by using an auxiliary segment which extends straight from one segment of plural digits arranged in the form of "8" and comprised of seven segments and is bent about at a right angle halfway, as shown in Figs. 12 to 14.

When the data imprinting mode selector switch 20 is turned on, the display section 38 recovers the current-date format which had been provided before it was switched into the PA mode, in whatever format the display has been.

By using the film exposed-frame number imprinting mode (FC mode), the interval timer mode and the PA mode in combination, it is possible to imprint information on the date and time, film frame number and the number of days selectively on the photos recorded on films at fixed intervals of time, so that the photography records and pictures will be very easily arranged.

Next, the input unit which receives the information from the camera body 46 through the serial interface circuit 19 in this embodiment of system will be described below.

In this embodiment, the data imprinting signal, the film frame counter information, and other camera information, etc. from the camera body 46 through the serial interface circuit 19 enter the input unit. As it is given in Table 1, the 16-bit serial data comprising D0 to D3 of 4 bits each is transferred from the camera body 46 in this transmission format. D0 and D1 are BCD codes corresponding to the higher place and lower place of 2 digits on the film frame counter respectively. D2 is the data imprinting signal and camera information. D2 is a data imprinting signal (also, a release signal) when bit 3 (MSB) is 1, and the data imprinting lamp lighting time may vary from t_0 to t_7 msec according to the values of the low order bits (bit 2, bit 1 and bit 0). When bit 3 in D2 is 0, the photography information mark (PIM mark) is turned on for bit 2 = 1 and turned

off for bit 2 = 0. If bit 3 is 0, the main switch 53 of the camera is in ON for bit 1 = 1 and in OFF for bit 1 = 0. If bit 3 is 0, the main switch 53 is latched in the previous state. D3 is 4 spare bits.

Table 1

D0	D1	D2	D3
MSB LSB	MSB LSB	MSB LSB	MSB LSB
****	****	****	****
High-order Place of 2 digits on counter	Low-order place of 2 digits on counter	Data imprinting signal and camera information	Spare bits

D2:

0XXX: No imprinting
1000: t_0 msec
1001: t_1 msec
1010: t_2 msec
1011: t_3 msec
1100: t_4 msec
1101: t_5 msec
1110: t_6 msec
1111: t_7 msec
01XX: PIM mark ON
00XX: PIM mark OFF
0X1X: Camera body main switch 53 ON
0X0X: Camera body main switch 53 OFF

Table 2-1 RAM

b_3 ... MSB of 4 bits
b_0 ... LSB of 4 bits
— ... not used

Address label	Contents
STATUS0	MSB = "1" ... Any display except for those in normal mode 3 low-order bits: = "000" ... Imprinting OFF mode = "001" ... "year/month/day" mode

= "010" ... "month/day/year" mode
= "011" ... "day/month/year" mode
= "100" ... "day/hour/minute" mode
= "101" ... Film frame counter mode

STATUS1 b_3 = 1 ... TRi port = H output state
b_2 = 1 ... Interval timer waiting state
b_1 = 1 ... Interval timer operating state
b_0 = 1 ... ——

STATUS2 b_3 = 1 ... Data modifying state
b_2 = 1 ... ——
b_1 = 1 ... Reference date setting state in PA mode
b_0 = 1 ... Interval timer time setting state

Table 2-2 RAM

Address label	Contents
STATUS3	b_3 = 1 ... ——
	b_2 = 1 ... ——
	b_1 = 1 ... LCD display change request flag
	b_0 = 1 ... ——
STATUS4	b_3 = 1 ... PA data imprinting mode in interval timer mode
	3 low-order bits:
	= "001" ... ——
	= "010" ... Reference date display in PA mode
	= "011" ... Time lapse display in PA mode
	= "100" ... Interval timer setting display
	= "101" ... Countdown display during the interval timer operation
STATUS5	b_3 = 1 ... REC port = H output state
	b_2 = 1 ... ——
	b_1 = 1 ... ——
	b_0 = 1 ... ——

Table 2-3 RAM

Address label	Contents
STATUS6	b_3 = 1 ... ———
	b_2 = 1 ... ———
	b_1 = 1 ... State that the interval timer time has been counted down to 10 sec or less
	b_0 = 1 ... iNT port in H output state
SECOND0	Low-order second digit of current time
SECOND1	High-order second digit of current time
MiNUTES0	Low-order minute digit of current time
MiNUTES1	High-order minute digit of current time
HOUR0	Low-order hour digit of current time
HOUR1	High-order hour digit of current time
DAY0	Low-order day digit of current date
DAY1	High-order day digit of current date
MONTH	Month number of current date
YEAR0	Low-order year digit of current date
YEAR1	High-order year digit of current date

Table 2-4 RAM

Address label	Contents
PDAY0	Low-order day digit of reference date in PA mode
PDAY1	High-order day digit of reference date in PA mode
PMONTH	Month digit of reference date in PA mode
PYEAR0	Low-order year digit of reference date in PA mode
PYEAR1	High-order year digit of reference date in PA mode
QDAY0	Low-order day digit of time lapse in PA mode
QDAY1	High-order day digit of time lapse in PA mode
QMONTH	Month digit of time lapse in PA mode

QYEAR0	Low-order year digit of time lapse in PA mode
QYEAR1	High-order year digit of time lapse in PA mode
TRXM0	Low-order minute digit of interval timer set-time
TRXM1	High-order minute digit of interval timer set-time
TRXH0	Low-order hour digit of interval timer set-time
TRXH1	High-order hour digit of interval timer set-time
TRSEC0	Low-order second digit on counter for interval timer
TRSEC1	High-order second digit on counter for interval timer
TRMiN0	Low-order minute digit on counter for interval timer
TRMiN1	High-order minute digit on counter for interval timer
TRHOUR0	Low-order hour digit on counter for interval timer
TRHOUR1	High-order hour digit on counter for interval timer

Table 2-5 RAM

Address label	Contents
SWX0	b_3 = 1 ... Switch 23 in pressed state
	b_2 = 1 ... Switch 22 in pressed state
	b_1 = 1 ... Switch 21 in pressed state
	b_0 = 1 ... Switch 20 in pressed state
SWY0	b_3 = 1 ... ———
	b_2 = 1 ... ———
	b_1 = 1 ... Switch 24 in pressed state
	b_0 = 1 ... Switch 25 in pressed state
SiO3B	Read D3 of serial data
SiO2B	Read D2 of serial data

SiO1B	Read D1 of serial data
SiO0B	Read D0 of serial data
SiOC	Read the rising pulse count of serial clock

Table 2-6 RAM

Address label	Contents
COUNT0	Counter to count 32Hz (for watch)
COUNT1	Counter to count 4Hz (for watch)
COUNT3	Counter to count 32Hz (for interval timer)
COUNT4	Counter to count 4Hz (for interval timer)
COUNT5	Counter to count 32Hz
COUNT6	Counter to count 4Hz
iNTCNT	Counter to count iNT port = H output time
FR0	Low-order digit on film frame counter
FR1	High-order digit on film frame counter

The contents of the data memory of the RAM 8 will be described below in reference to Table 2, where the address label and the contents are placed left and right respectively.

In STATUS0, b_3 (MSB) = 1 indicates any other displays, such as PA mode and interval timer displays, than normal data imprinting displays. The 3 low-order bits, b_2, b_1 and b_0, indicate normal data imprinting mode; imprinting OFF mode for "000", "year/month/day" mode for "001", "mont/day/year" mode for "010", "day/month/year" mode for "011", "day/hour/minute" mode for "100" and film frame counter imprinting mode for "101".

In STATUS1, b_3 = 1 indicates the TRi port = high (H) level output state. b_2 = 1 indicates that the

interval timer has delivered the signal iNT port = H level and is in waiting state until it receives the status signal of the main switch 53 from the camera body 46. b_1 = 1 indicates the interval timer countdown operation. b_0 is not used.

In STATUS2, b_3 =1 indicates that any data is being modified by the switches 21 to 23 as shown in Fig. 1. b_2 = 1 is not used. b_1 = 1 indicates the reference date setting state in PA mode. b_0 = 1 indicates that the interval timer is in time setting state.

In STATUS3, b_1 = 1 indicates the flag which requests to display the LCD presentation changed. b_3, b_2 and b_0 are not used.

In STATUS4, b_3 = 1 indicates the PA mode data imprinting in interval timer mode. The 3 low-order bits, b_2, b_1 and b_0, are used to specify the display mode and the display type; reference date display in PA mode for "010", time lapse display in PA mode for "011", interval timer setting display for "100" and interval timer countdown display for "101".

In STATUS5, b_3 = 1 indicates that the REC port is in high (H) level state. b_2, b_1 and b_0 are not used.

In STATUS6, b_1 = 1 indicates that the interval timer has counted down the time to 10 sec or less. b_0 = 1 indicates iNT port = H level output state. b_3 and b_2 are not used.

SECOND0 to YEAR1 store the low-order second digit to the high-order year digit of the current date

and time. PDAY0 to PYEAR1 store the low-order day digit to the high-order year digit of reference date in PA mode.

QDAY0 to QYEAR1 store the low-order day digit of the time lapse to the high-order year digit of the time lapse.

TRXM0 to TRXH1 indicate the low-order minute digit to the high-order hour digit of the interval timer set time respectively. TRSEC0 to TRHOUR1 indicate the low-order second digit to the high-order hour digit of the interval timer countdown counter respectively.

In SWX0, b_3 = 1 indicates the switch 23 being in pressed state, b_2 = 1 the switch 22 in pressed state, b_1 = 1 the switch 21 in pressed state, and b_0 = 1 the switch 20 in pressed state.

In SWY0, b_1 =1 indicates the switch 24 being in pressed state, and b_0 = 1 the switch 25 in pressed state. b_3 and b_2 are not used.

SiO3B to SiO0B read and store the 4-bit of each of D3 to D0 of the serial data respectively.

SiOC is a counter which counts the clocks as the serial codes enters it, and is reset when the buffers (SiO3B, SiO2B, SiO1B and SiO0B) complete the reading of said serial codes (D0, D1, D2 and D3).

COUNT0 and COUNT1 are 32 Hz and 4Hz counters for the watch. COUNT3 and COUNT4 are 32Hz and 4Hz counters respectively for the interval timer. COUNT5 and COUNT6 are auxiliary 32Hz and 4Hz counters

respectively. iNTCNT is a counter which counts the iNT port output time with each interrupt signal 32HziNT when the iNT port is in H level state.

FR0 and FR1 store the low-order and high-order digits in the film frame counter imprinting mode, respectively.

Now, the sequential operation of the microcomputer will be described below in reference to Figs. 15A to 15D and Figs. 16A to 16R, flow charts illustrating the software.

Figs. 15A to 15D are the schematical flow charts of the program. This program is roughly divided in 4 blocks. The first block is for initialization, as shown in Fig. 15A. This block is used to clear the memory areas, to set the first display data and to adjust the display after the microcomputer has been powered on the reset. After the initialization was completed, the CPU 1 becomes in HALT state where the stored data are held in it. As shown in Fig. 15B, 32HziNT is a processing sequence for the interrupt signals which are produced at the rate of 32 signals per second with the 32Hz pulses transmitted by the frequency dividing circuit 5 as shown in Fig. 3. This sequence is used to monitor the switches 20 to 25 and process said signals in response to the pressed state of the switches 20 to 25, and to produce a carry signal of 1 second for incrementing the watch and calendar, when 32 interrupt signals are counted up. As shown in Fig. 15C, SiOiNT is a processing sequence

for the serial interrupt signal which is produced when the CPU 1 receives the serial codes from the camera body 46, and it is used to process the input of the data imprinting lamp lighting and camera information. RTiNT as shown in Fig. 15D is a processing sequence for the timer interrupt signal which is generated when the TRi timer counts up, and it is used to process the data imprinting lamp lighting end time.

This embodiment according to the present invention will be described in detail in reference to the flow charts Figs. 16A to 16R.

When the power supply 2 is turned on, the microcomputer is initially reset with the reset (RE) signal produced by the PUC circuit 3, and starts to operate from the program step #001 as shown in Fig. 16A. All the memory areas are cleared on Step #002, the data imprinting mode is switched from the initial display to the "year/month/day" mode on Step #003, and the calendar date is set, for example, to "January 1, 87" on Step #004. On Step #005, the stack pointer area is cleared. The interruption is enabled on Step #006, and the microcomputer becomes in HALT state, that is, data holding state, on Step #007.

When the CPU 1 receives an interrupt signal 32HziNT, the microcomputer starts in operation from Step #101, as shown in Fig. 16B. On Steps #101 and #102, the states of the switches 20 to 2d5 are read through the switch input port. Then, on Steps #104, #105, #106,

#107, #108, and #109 (#108 and #109 are shown in Fig. 16F), it is determined whether the states of the switches 20 to 25 are changed or not, and if any change is detected, the required processing is made. The detailed information on this processing will be given hereinafter. If any switch is not changed in state, the control proceeds from Step #109 to Step #201 (Fig. 16G).

Here, the case will be described that all the switches are pressed down.

At first, the case that the switch 20 is pressed down will be described below.

If the pressed state of the switch 20 is detected on Step #104, the control proceeds to Steps #129, #130, #131, #133, #134 and #135, and to Step #201. If it is detected on Step #129 that the time lapse display in PA mode is provided, or if it is detected on Step #130 that the time has been counted down to 10 seconds in timer mode, the subroutine RTCANCL is called on Step #132 to cancel the PA mode or the timer mode. If the time is not counted down to 10 seconds, it is determined on Step #131 whether the display is in normal mode or not. If the display is not in normal mode, the subroutine RTCANCL is called on Step #132 as if the time is counted down to 10 seconds in timer mode. The processing of the subroutine RTCANCL to cancel the timer will be described hereinafter. When the timer cancel subroutine has been processed, the control proceeds to Step #201.

If it is detected on Step #131 that the display is in normal mode, STATUS0 is incremented by 1 on Step #133 to advance the data imprinting mode by one. If STATUS0 = 6 is detected on Step #134, STATUS0 = 0 is provided on Step #135, where 6 normal data imprinting modes, "year/month/day" → "month/day/year", → "day/month/year" → "day/hour/minute" → "FC mode" → "imprinting OFF mode", and cycled.

The case that the switches 21, 22 and 23 are pressed down will be described below.

If it is detected on Step #105 that the switch 21 is changed in state, the changed state of the switch 21 is determined on Step #105A. If the switch 21 is in pressed state, b_3 = 1 (data modifying state) in STATUS2 is set on Step #140, and b_1 = 1 in STATUS3 display change request flag) is set on Step #141 to update the display because of its contents changed. Then, on Step #142, it is determined which data is corresponding to the switch 21 according to the detection of the values in STATUS0 and STATUS4, and the corresponding data is modified. The detailed information will be provided hereinafter. After the modification has been completed, the control proceeds to Step #201.

If it is detected on Step #105A that the switch 21 is in OFF after the state was changed, b_3 = 0 in STATUS2 is set to reset the data modifying state, and b_1 = 1 in STATUS3 (disply change request flag) is set on Step #144. the states of the switches 22 and 23 are

determined for any change on Steps #106 and #107 respectively, and subsequently processed as the state of the switch 21 is. Therefore, the processing of the switches 22 and 23 is not described here. After the modification has been completed, the control proceeds to Step #201 for the switches 22 and 23.

If the switch 24 is pressed down (see Fig. 16F), it is detected on Step #108 that the switch 24 is changed in state, and the changed state of the switch 24 is determined on Step #160. If it is detected that the switch 24 is in ON, the subroutine RTCANCM is called on Step #170. The subroutine RTCANCM will be described hereinafter. STATUS2 is set to PA mode reference date setting state on Step #171, and set to PA mode reference date display state on Step #172. On Step #173, the subroutine EXTDSP is called to control the displays in other modes than in normal mode. Then the control proceeds to Step #201.

If it is detected on Step #160 that the switch 24 is in OFF after changed in state, it is determined on Step #161 whether it is in PA mode reference date setting state or not. If it is in setting state, the PA mode time lapse display mode is set on Step #162, and $(STATUS2)_1 = 0$ is set on Step #163 to cancel the PA mode reference date setting state. Then, the control proceeds to Step #201.

If the switch 25 is set in pressed state, the change of the switch 25 is detected on Step #109, and

the changed state of the switch 25 is determined on Step #110. If the switch 25 is in ON, it is determined on Step #111 whether the interval timer has been operated or not. If it is detected that the interval timer has not been operated, it is determined on Step #112 whether the interval timer is in timer time setting state. If the interval timer is not in time setting state, the control proceeds to Step #121 and then the Step #201. On Step #121, the subroutine TRMS is called to process the interval timer mode setting.

Here, the setting process in interval timer mode will be described in reference to Fig. 16K.

On Step #151, STATUS is set into the interval timer time setting state. On Step #152, all the digit places, low-order second place to high-order hour place, of the counter watch for the timer are cleared to zero (0). On Step #153, the subroutine EXTDSP is called to process the displays in other modes than in normal mode. This subroutine will be described hereinafter. On Step #154, it is determined if the data imprinting mode in interval timer mode is PA mode or not. If the data imprinting mode is not PA mode, it is determined on Step #155 whether the display is PA mode time lapse display or not. If it is time lapse display, bit 3 and 2 in STATUS4 are set on Step #156 to PA data imprinting mode and interval timer setting state respectively. If bit 3 in STATUS4 is detected to be set on Step #154, the same operation is provided. If it is detected on Step

#155 that the imprinting mode is not PA mode, the interval timer setting display state is set on Step #157.

After the interval timer mode setting has been completed, the control proceeds to Step #201. If the interval timer time setting state is detected on Step #112, the control proceeds to Steps #113 and #114, and the interval timer starts in operation. On Step #113, the subroutine iNTACT is called to set the iNT port into active state. The subroutine iNTACT starts from Step #731 (Fig. 16R). The signal iNT port = H is outputted on Step #731. On Step #732, the initial value of the iNTCNT counter for counting iNT port output time is set, and the flag of iNT port = H output is set on Step #733.

Next, the flag of interval timer time setting state is reset on Step #114, and on Step #115, it is determined whether all the digits in the interval timer are zero or not. If all the digits are zero, since the interval timer time has not been set, the interval timer is brought into a state of 10 second before counting up on Step #116 so that the self-timer of the camera body is used as the interval timer. The control comes into a state of waiting to receive a data imprinting signal from the camera body. On the other hand, if it is determined on Step #115 that the interval timer time is not zero, STATUS is set into a state of waiting to receive a main switch state signal (in serial code) from the camera body on the startup of the interval timer. The low-order and high-order second digit places of the

interval timer are cleared to zero (0) on Step #116B. On Step #117, the interval timer operating state is set, and on Step #118, the display change request flag is set. On Step #119, the interval timer set time of low-order minute digit to high-order hour digit, which was stored on the startup of the timer, is copied in the RAM area which counts it down. Subsequently, the control proceeds to Step #201.

How to determine modes and modify data, if the switches 21, 22 and 23 are pressed down, will be described below in detail in reference to Figs. 16C, 16D and 16E.

At first, the modification by the switch 21 will be described. In Fig. 16C, on Step #800, it is determined whether MSB in STATUS0 is set or not, and if it is set, it indicates any display in non-normal mode. If the display is detected on Step #801 to be in PA mode and in form of "month/day/year", the switch 21 corresponds to the place "month". As the result, the "month" place PMONTH of the time lapse reference date is incremented on Step #804. If the display mode is "day/month/year", the switch 21 corresponds to "day". Then, the "day" PDAY of the time lapse reference date is incremented on Step #805. If the display format is not "month/day/year" nor "day/month/year", the format "year/month/day" is selected as reference date display format in PA mode. Then, the switch 21 corresponds to the place "year", and the "year" PYEAR is incremented

on Step # 803. If the normal display mode is detected on Step #800, Step #806, #807, #808 or #809 is used to determine and detect the display mode, and the digit place corresponding to the switch 21 is incremented on Step #811, #812, #813 or #814 respectively, as it is in PA mode.

Next, the modification by the switch 22 will be described below. In Fig. 16D, the display is judged to be in non-normal mode if it is detected on Step #820 that MBS in STATUS0 is set, as it is in case of modification by the switch 21. if it is detected on Step #821 that the display is in interval timer time setting mode, the switch 22 corresponds to the place "hour" of the timer time setting display, and the "hour" TRXHOUR is incremented on Step #825. On Steps #823 and #826, or on Steps #823 and #824, the modification of the PA mode reference date digit corresponding to the switch 22 is similar to that for the swtich 21.

If the normal display mode is detected on Step #820, the display mode is determined and detected on Step #827, #828, #829 or #830, and the digit corresponding to the switch 22 is incremented on Step #831, #832, #833 or #834 respectively, as it is in case of the switch 21.

Finally, the modification by the switch 23 will be described below, in reference to Fig. 16E. If the interval time time setting mode is determined and detected on Steps #840 and #841, the timer minute digit

(TRXMiN) corresponding to the switch 23 is incremented on Step #845, as it is in case of the switch 22. If the display is in normal mode, the display mode is determined on Step #847, #848, #849 or #850, and the digit corresponding to the switch 23 is incremented on Step #852, #853, #854 or #855 respectively, as it is in case of the witches 21 and 23.

After the monitor processing of the switches 20 to 25 has been completed, as described above, the 32Hz interrupt process is followed by the watch increment process and the timer countdown process on Steps #201 and subsequent (see Fig. 16G).

On Step #201, it is determined whether the iNT port is in active state or not. If the iNT port is active, the iNT port output time counter iNTCNT is decremented by 1 on Step #202, and it is determined if iNTCNT = 0 or not on Step #203. If iNTCNT = 0, the subroutine iNTSTP is called on Step #204 to provide iNT port = L. The iNTSTP subroutine will be described by using Steps #751 and subsequent in Fig. 16R.

iNT port = H is set on Step #751, and iNT port in active state is canceled on Step #752. The iNT port output time is 1/32Hz x 7 = 218 msec, because the initial value of the iNTCNT is 7.

Steps #205 to #210 are for the increment process of the data imprinting watch and calendar. The 32Hz counter COUNT0 for watch is incremented on Step #205. If COUNT0 = 8 is detected on Step #206, a 4Hz carry is

outputted to increment the 4Hz counter COUNT1 by 1 on Step #207 and at the same time, to clear COUNT0 to zero (0) on Step #207A. On Step #208, COUNT1 = 4 is checked. If it is 4, a carry signal of 1 second is delivered on Step #209, and the watch and calendar are incremented on Step #210. It is determined on Step #211 whether the timer is operating or not. If the timer is operating, REC port = H output state is not checked on Step #212. This means that in addition to the above-described watch counter, 32Hz and 4Hz counters used on Steps #213 and #215 are separately provided to count down the timer set time during the interval timer operation and to count the output time of the data imprinting recognition mark (REC port) during the output thereof, so that the control will jump to Steps #250 and subsequent without passing Steps #213 and subsequent for counting, if the interval timer is not operating or if REC port = H output state is not detected. If the interval timer is operating or if REC port = H output state is detected, another 32Hz counter COUNT3 separately provided from the above-described COUNT1 is incremented by 1 on Step #213, and it is determined on Step #214 whether COUNT3 = 8 is true or not. If COUNT3 = 8 is true, a 4Hz carry signal is produced to increment the 4Hz counter COUNT4 on Step #215 as shown in Fig. 16H and to clear the 32Hz counter COUNT3 to zero (0) on Step #216. On Steps #218 and #219, it is then determined whether the contents of the counter COUNT4 is 4 or more. if it is 4 or more, the timer

produces a carry signal or 1 second. In these conditions, it is determined on Step #220 whether the interval timer is operating or not. If the interval timer is operating, it is determined on Step #221 whether the interval timer is or not in main switch state signal (in serial code on timer startup) input waiting state. If the timer is not in waiting state, the control proceeds to Step #222 where the display change request flag is set, and to Step #223 where the subroutine RLTiMER is called to process the countdown operation of the interval timer. The subroutine RLTiMER will be described below by referring to Fig. 16J. The subroutine RLTiMER starts the processing on Step #301. Since the timer counter produced a carry signal of 1 second on Step #219, the low-order second digit TRSEC0 on the interval timer is decremented by 1 on Step #301, and the low-order second digit is checked for 0 on Step #302. If it is zero (0), the high-order second digit is decremented by 1 on Step #303. On Step #304, it is detemined whether the zero flag is set or not on the microcomputer as the result that the high-order second digit was decremented on Step #304. If the zero flag is set, the minute digits, and the hour digits if the zero flag is set as the calculating result of the minute digits, are sequentially decremented on Step #305. On Steps #306, 307 and #308, it is checked if the minute digits = 0, hour digits = 0, and high-order second digit = 1 and low-order second digit = 0 are true or not, that is, if the interval timer is 10 seconds

before it counts up. If the timer is 10 seconds before counting up, the subroutine iNTACT is called to make the above-described iNT port active on Step #309. Since the control is arranged as described above, if the self-timer of the camera body is set, for example, in 10 seconds, the time left, 10 sec, is checked at this point, and the self-timer of the camera body starts in counting by setting the iNT port on H level.

On Step #310, STATUS is set in the state that the interval timer time has been counted down to 10 seconds or less. On Step #311, it is determined whether the imprinting mode is the normal mode or the PA mode. If it is determined to be the PA mode, the imprinting display is set to the time lapse display on Step #313. On the other hand, if it is determined to be the normal mode, MSB in STATUS0 is made to be zero on Step #312, so that the imprinting display is set to the normal imprinting display. Accordingly, the interval timer countdown display is switched again to the data imprinting information display. On Step #314, the subroutine MDCLR is called to clear the data display area, since the display mode was changed. The subroutine MDCLR is processed on Steps #395 and #396 as shown in Fig. 160. The display change request flag is set on Step #395, and blank signals are transmitted to all display digit places on Step #396 to clear the display area. On the other hand, if not TRSeC1 = 1 on Step #307, all the digits of the timer are judged again on Step #315. If all the

digits are zero, the timer is in the state of counting up, so that on Step #316 an operating state of the interval timer is cancelled.

On Step #225, it is checked if the 4Hz counter COUNT4 is 8 or more. If this counter is 8 or more, a carry of 2 seconds is produced on Step #226. If the data imprinting recognition mark output state (REC port = H) is detected on Step #227, REC port = L is set on Step #228 to turn off the REC mark 37. On Step #229, STATUS5 is reset to data imprinting REC mark output state flag. Then, COUNT0 = 0 is checked on Step #250 (Fig. 16I). If it is not 0, the display change request flag is checked on Step #251. If this flag is set, the display mode is determined according to the values of STATUS0 and STATUS4 on Step #259, and the display information according to the mode is transmitted to the LCD driver 9. On Step #260, the display change request flag is reset, and on Step #280, the CPU 1 is set in HALT state. If COUNT0 = 0 is detected on Step #250, a 4Hz carry signal is produced. On Step #252, it is determined whether the interval timer time has been counted down to 10 seconds or less. If it has been counted down within 10 seconds, it is checked on Step #253 if the interval timer is counting down or not. If the timer is not operating, the interval timer is in the state of counting up, similar to that on Step #315, so that the low-order second digit TRSEC0 on the timer is incremented by 1 on Step #254. On Step #255,

TRESEC0 = 8 is checked. If it is 8, the high-order second digit of the timer is incremented by 1 on Step #256, and at the same timer, TRSEC0 is cleared to 0 on Step #256A. On Step #257, it is determined whether TRESEC1 is 10 or more. If it is 10 or more, it means that 20 seconds or more (4Hz x 80 counts) have passed after the timer counted up. Consequently the subroutine RTCANCM is called on Step #258 to cancel the interval timer. The subroutine RTCANCM will be described hereinafter. After the interval timer was canceled, the mode is checked according to the values of STATUS0 and STATUS4, and the display according to the mode is provided on Step #259. Then, the CPU 1 is set in HALT state. If the display change request flag is not set on Step #251, the display information is not changed, and the CPU 1 is set in HALT state.

The processing of the serial codes received from the camera body will be described below by referring to Fig. 16L.

When the CPU 1 receives the serial interrupt signal, the program starts to process Step #501 "SiOiNT". On Step #501, it is determined if the contents of the dSiCNT counter which counts the pulses of serial synchronous clocks is 16. If it is not 16, the serial input data are considered to be invalid on Step #540, and the CPU 1 is set in HALT state. If the clock count is 16 with the data valid, the contents of each serial buffer, which are 16-bit serial data divided into 4 groups

of 4 bits each, are loaded in the RAM areas SiO0, SiO1, SiO2 and SiO3 on Step #502, and the SiCNT counter is cleared to 0 on Step #503. On Step #504, the bit 3 (MSB) in SiO2 is checked. If the state of bit 3 is 1, it indicates the data imprinting signal (also, the release signal), and the subroutine LAMPON for lighting the data imprinting lamp 14 is called on Step #550. Now, the processing of this subroutine LAMPON will be described below in reference to Fig. 16M. On Steps #601, #602 and #603, it is checked if the lamp has been lighted (TRi port = H), if the data is being modified by the modifying switches and if the PA mode reference date is being set (the switch 24 is in pressed state) respectively. If any of these states is detected, the lamp lighting state is disabled to turn off the lamp. Then, on Step #604, it is checked if STATUS is in the state that the interval timer has been counted down within 10 seconds. If STATUS is in the state, it is determined on Step #630 whether the data display mode is OFF mode. If it is OFF mode, the subroutine PHOTOEND is called on Step #631 to prepare for starting the next counting process of the interval timer. If the display mode is not OFF mode, the control proceeds to Steps #608 and subsequent for the lamp lighting process.

Here, the subroutine PHOTOEND will be described in reference to Fig. 16N. In PHOTOEND, the low-order and high-order second digits on the interval timer counter are cleared to zero (0) on Step #661. On jStep #662,

the low-order minute digit to high-order hour digit of the interval timer set time stored on the startup are copied in the memory area which counts down in practice. On Step #663, the subroutine EXTDSP is called to process the other displays than the data imprinting information display.

The subroutine EXTDSP starts on Step #350 as shown in Fig. 16P. On Step 351, STATUS is set in displaying state in any other mode than in normal mode. On Step #352, the display change request flag is set, since the display mode is changed. On Step #353, blank signals are transmitted to the digit places of the display area to clear the displayed digits.

After EXTDSP has been processed, the STATUS6 which is in the state that the interval timer has been counted down within 10 seconds is reset on Step #665. On Step #666, the flag of interval timer countdown operation is set. On Step #667, it is checked if the data imprinting mode is PA or time lapse display mode. If it is time lapse mode, the control proceeds to Step #668 where STATUS is set to interval timer mode and PA mode and where the flag for countdown display during the timer operation is set. If it is detected on Step #667 that the data imprinting mode is not PA mode, only the flag for timer countdown display is set on Step #669. Thus, the PHOTOEND process is completed and the control returns to the the subroutine LAMPON. If the data imprinting mode is OFF mode, the CPU 1 is set in HALT

state after having returned from the subroutine LAMPON.

If it is not detected on Step #604 in the subroutine LAMPON that the interval timer has counted down within 10 seconds, it is checked on Steps #605 and #606 if STATUS is in interval timer counting state and in interval timer time setting state respectively. If STATUS is in any of the two states, the interval timer mode cancel process is performed on Steps #620 and subsequent. This process will be described hereinafter. If STATUS is not detected on Steps #605 and #606 to be in any of said two states, it is determined on Step #607 whether the data imprinting mode is OFF mode or not. If OFF mode is detected, the CPU 1 exits the data imprinting lamp lighting process and enters the HALT state. If OFF mode is not detected on step #607, the control proceeds to Step #608 where the TRi timer time is set according to the values of the 3 low-order bits in SiO2 and where the timer counting is started. Then, TRi port = H is set on Step #609 to start the lighting of the lamp 14. On Step #610, STATUS is set to TRi port = H output state. The REC mark 37 is lighted on Step #611, and REC port = H output state is set on Step #612. Thus, the lamp lighting process is completed. Then, the control teturns to SiOiNT and the CPU 1 is set in HALT state.

If it is detected on steps #605 and #606 that the interval timer is in operating state or in time setting state respectively, it is checked on Step #620

if STATUS is in interval timer mode and in PA data imprinting mode. Thus, the interval timer cancel means are divided into two. At first, if the interval timer is in PA mode, that is, if MSB of STATUS4 is 1, the subroutine RTCANCM is called on Step #621. In the subroutine RTCANCM as shown in Fig. 160, the flag of interval timer operating state is reset on Step #391, and the flag of interval timer time setting state is reset on Step #392. Then, the flag of interval timer having counted down within 10 seconds is reset on Step #393. The control returns to Step #622.

On Step #622, the display after the interval timer was canceled is changed into the PA mode timer lapse display. Since the display is changed, the display change request flag is set on Step #623. On Step #624, the above-descried subroutine MDCLR is called to clear the display area, and the CPU 1 exits the subroutine LAMPON. If it is detected on Step #620 that MSB of STATUS4 is 0, that is, that the data imprinting mode is not PA mode, the subroutine RTCANCL is called on Step #640 to cancel the interval timer mode. In the subroutine RTCANCL as shown in Fig. 160, STATUS is returned to the data imprinting information display in normal mode by resetting MSB of STATUS0 on Step #381. At this point, if the interval timer mode or PA mode were recovered to set MSB in STATUS0, the values in the 3 lower-order bits would not be changed. If the interval timer mode or PA mode were canceled to reset MSB of STATUS0,

therefore, the state (display) in interval timer mode or PA mode, which had been provided before the interval timer mode or PA mode was set, could be recovered by checking the values in the 3 lower-order bits. The subroutine RTCANCL is thus designed. The subroutine RTCANCL then jumps to the subroutine RTCANCM where each STATUS flag in interval timer mode is reset, as described above. The CPU 1 exits the subroutine LAMPON and enters in HALT state.

Here, the SiOiNT interrupt process will be described below in reference to Fig. 16L. If the lamp lighting signal is not detected on Step #504, the PIM port is set to "H" or "L" on Step #506 or #507 respectively according to the state of bit 2 in SiO2 detected on Step #505. On Step #508, the state of bit 1 in SiO2 is detected, and the process depends upon the state of the main switch 53 on the camera body. If the main switch 53 is set in ON, it is determined on Steps #509 and #510 whether STATUS is or not in interval timer operating state and in a waiting state to receive a main switch state signal (in serial code) from the camera body. If STATUS is in the waiting state, the low-order and high-order second digits on the timer counter are cleared to zero (0) on Step #511, the waiting state of STATUS is reset on Step #512, and the interval timer is set into interval timer operating state so that the interval timer can start counting down from the next 32Hz interrupt. To inform the camera body of the waiting

state end, the subroutine iNTSTP is called on Step #514 to set iNT port = L. Then, the CPU 1 enters in HALT state.

In the subroutine iNTSTP, as shown in Fig. 16R, the I/O port 17 delivers iNT port = L on Step #751, and the iNT port active flag is reset on Step #752.

If it is detected on Step #508 that the main switch 53 is in OFF, it is checked on Step #515 if the interval timer is operating. If it is operating, the interval timer cancel process is divided into two courses according to the data imprinting mode which is PA mode or not; Steps #516, #517, #518, #519 and #520 and Steps #516 and #530, as Steps #620, #621, #622, #623 and #624 and Steps #620 and #640 in the above-described subroutine LAMPON as shown in Fig. 16M. After the interval timer cancel process has been completed, the CPU 1 enters in HALT state.

Next, the timer interrupt process (RTiNT) required on the TRi timer counting up will be described in reference to Fig. 16Q.

If the timer interrupt occurs, the CPU 1 starts the operation from Step #701. On Step #701, TRi port = L is set to turn off the lamp. On Step #702, STATUS of TRi port = H output state is cleared. It is then determined on Step #703 whether the interval timer time has been counted down within 10 seconds or not. If the time left is not within 10 seconds, the RTiNT process is completed to set the CUP 1 in HALT state. If it is

detected on Step #703 that the interval timer time has been counted down within 10 seconds, the subroutine PHOTOEND is called on Step #704 to prepare for the next counting cycle of the interval timer. The subroutine PHOTOEND is as described in the SiOiNT process. On Step #705, the subroutine EXTDSP is called to process the other displays than the data imprinting information display in normal mode. The subroutine EXTDSP is as described above. Then, the sequence is set in HALT state.

Here, how to monitor the state of the main switch 53 on the camera body on the startup of the interval timer will be described below.

During the interval timer operation, the camera is released by the self-timer started up. Therefore, the camera control circuit is required to identify (i) the timer startup signal, (ii) the timer release signal and (iii) the self-timer startup by a self-switch. Fig. 17 shows the circuit configuration of the connection between the iNT port terminal of the interval timer and the SELF terminal of the camera control circuit in this embodiment according to the present invention. In this figure, the configuration of the interval timer control circuit is shown in the box defined by a broken line on the left side, while the configuration of the camera control circuit is shown on the right side.

In this figure, 40 is an iNT terminal in the interval timer control circuit 43, which is described hereinafter. 41 is an N-channel MOS transistor, which

is the same as shown by 18 in Fig. 3. 42 is an iNT signal output buffer, 43 is an interval timer control circuit which contains the above-described microcomputer, 50 is a self-timer switch on the camera, 55 is a SELF terminal in a camera control circuit, 56 is a SELF signal input inverter, 57 is a resistor which pulls up the input to the inverter 56, and 58 is a camera control circuit.

Now, the signal timings will be described by referring to the timing charts, Figs. 18A to 18C. If the self-timer is started up by means of the self-timer switch 50, the input to the inverter 56, which has been pulled up by the pull-up resistor 57, is set to L level when the self-timer switch 50 is turned on, as shown in the timing chart, Fig. 18C. The camera control circuit 58 is designed so that it can sample the SELF terminal 55 at the predetermined period of timer (T), for example, that the self-timer is started up when 2 or more L levels are detected. The camera control circuit 58 is also designed so that it can transfer the serial code containing the main switch state signal to the interval timer through the above-described serial interface circuit 19 when it samples and detect the first L level of the SELF terminal. Therefore, the self-timer on the camera can be started up by pressing the self-timer switch 50 for a longer time than the sampling period (T).

As it is shown in the timing chart, Fig. 18A, when the interval timer is started up, the interval timer control circuit 43 sets the MOS transistor 41 to ON to

set the SELF terminal 55 to L level, and the camera control circuit 58 then detects L level of the SELF terminal 55 for the first timer by sampling and delivers the main switch state signal in serial code. The interval timer control circuit 43 receives this state signal and sets the iNT port to L level at the same time. If this setting of the iNT port to L (SELF terminal = H) occurs before the second sampling of the SELF terminal, the self-timer on the camera body will not start up. Since the interval time control circuit 43 side has received the state signal of the main switch 53 in serial code, it can determine whether the interval timer is to be started or not, by checking the serial code. The checking process is as described in the explanation on SiOiNT as shown in Fig. 16L.

Finally, if the interval timer counts up to start the self-timer, the interval timer control circuit 43 does not set the iNT port to H according to the serial code input, but keeps it on "L" level for the predetermined timer (200 msec in this embodiment), unlike the above-described starting, as shown in the timing chart Fig. 18B, and can start up the self-timer when the 2 "L" levels of the SELF terminal are detected. It is understood that the sampling period (T) for the SELF terminal in the camera control circuit 58 is sufficiently shorter than 200 msec.

In this embodiment, the interval timer mode is canceled if the main switch 53 on the camera body

is in OFF. However, the timer time may be reset in interval timer mode.

Alternatively, this embodiment may be disgined so that a warning display can be provided if the main switch 53 on the camera body is in OFF when the interval timer is started, or if the main switch 53 on the camera body is set to OFF during the operation of the interval timer.

Fig. 19 is a block diagram showing the circuit configuration of another timer unit for use in the present invention, comprising a data imprinting capability mounted on the camera, as in the above-described embodiment.

In Fig. 19, 101 is a central processing unit (hereinafter referred to as CPU) which calculates any lapsed time and controls the operating sequence of the circuits as described hereinafter. 102 is an oscillator circuit. 103 is a frequency dividing circuit which divides the output from the oscillator circuit 102 and delivers clock pulses at the predetermined period to the CLK terminal of the CPU 101. 104 is a memory RAM and 105 is a memory ROM. 106 is a day pulse generating circuit which divides the clock pulse output signal from the frequency dividing circuit 103 to produce a day pulse which represents a day.

The memory 104 inputs and outputs data. The

memory 105 stores the contents of a program.

In the upper part of Fig. 19, a block A defined by a broken line represents a current-date counter which counts the current date and contains a current-year counter circuit 107, a current-month counter circuit 108, a current-day counter circuit 109, a leap-year determining circuit 110 and an "end of month" correcting circuit 111.

The current-year counter 107 delivers an output corresponding to the 2 lowest-order digits of the current year in the Gregorian calendar to the input ports Y0 to Y5 in the CPU 101.

The current-month counter 108 delivers an output corresponding to the number of the current month (which is represented by any of the numbers 1 to 12 corresponding to January to December respectively) to the input ports M0 to M3 in the CPU 101.

The current-day counter 109 delivers an output corresponding to the current day to the input ports D0 to D4 in the CPU 101.

The leap-year determining circuit 110 is a known circuit which determines whether the output from the current-year counter 107 corresponds to a leap-year or not.

The "end of month" correcting circuit 111 determines whether the output from the current-month counter 108 corresponds to the current month of 31 days or 30 days and whether the output from the current-year

counter 110 corresponds to the leap-year or not if the current month is determined as February (containing 29 days in a leap-year or 28 days in any other year), and delivers an "end of month" correcting signal to the current-day counter 109.

In the upper and right part of Fig. 19, a block B represents a reference date setting counter which sets the reference date for the calculation of a lapsed time. This counter contains a reference year counter 112, a reference month counter 113, a reference day counter 114, a leap-year determining circuit 115 and an "end of month" correcting circuit 116.

The reference year counter 112 counts years in the Gregorian calendar, the reference month counter 113 counts months, and the reference day counter 114 counts days. The reference year counter 112 delivers the output to the input ports SY0 to SY5 in the CPU 101. The reference month counter 113 delivers the output to the input ports SM0 to SM3 in the CPU 101. The reference day counter 114 delivers the output to the input ports SD0 to SD4 in the CPU 101. The "end of month" correcting circuit 116 delivers the output to the input ports DM0 to DM4 in the CPU 101.

The "end of month" correcting circuit 116 produces an "end of month" correction signal which commands the CPU 101 to correct the day count from the reference day counter 114 as well as the 5-bit information of the days in the reference month, and delivers the

signal and the 5-bit information to the input ports DM0 to DM4 in the CPU 101.

The current-year counter 107, the current-month counter 108, the current-day counter 109, the reference year counter 112, the reference month counter 113 and the reference day counter 114 are arranged to be controlled by the data correction pulse signal produced by a data correction pulse generating circuit 117. This circuit 117 selects one of the above 6 counters when a switch 118 connected to the circuit 117 is closed, and applies a correction increment pulse to the selected counter when a switch 119 connected to the circuit 117 is closed.

In the lower and left part of Fig. 19, a block C represents a display means which displays a lapse of time from any reference time to the current time in addition to the other data. The display means contains decoders 121 to 123 and display sections 124 to 127. The decoder 121 decodes the high-order two digits of the time lapse data produced by the output ports PH0 to PH5 in the CPU 101, and delivers its output to a driving element to drive 2 display elements of 7 segments each in the high-order digit display section 124. The decoder 122 decodes the low-order two digits of the time lapse data produced by the output ports PL0 to PL4 in the CPU 101, and delivers its output to a driving element to drive 2 display elements of 7 segments each in the low-order digit display section 125. Therefore, the

decoders 121 and 122 have 7 output ports SH0 to SH6 and SL0 to SL6 respectively for each display element in the display sections 124 and 125 respectively.

The decoder 123 produces the driving outputs corresponding to the units (year, month and day) for any lapsed period of time, and delivers them to the unit display sections 126 and 127. This decoder 123 decodes the output signal produced by the output port YM/MD CTRL in the CPU 101, and delivers through 2 output ports C0 to C2 the output to a driving element to drive the display element of segments corresponding to the high-order data (y or m, that is, year or month respectively) as well as the output to a driving element to drive the display element of segments corresponding to the low-order data (m or d, that is, month or day).

130 is a driver circuit which drives an LED 131 which displays a warning according to the output from an output port WARN in the CPU 101, if the reference date is set on or after the current date.

Fig. 20 is a table listing the port addresses and their contents in every input or output port in the CPU 101 in reference with every memory address.

Fig. 21 is a table listing the outputs (DM outputs) of the "end of month" correcting circuit according to the reference year and the reference month.

Fig. 22 is a flow chart showing a program run in the CPU 101.

Fig. 23 is a schematical view showing the

configuration of the decoder 123, the layout of segments in the unit display sections 126 and 127, and the electrical connections of the segments with the decoder 123.

The contents of the current-year counter 107, the current-month counter 108 and the current-day counter 109 as well as the contents of the reference year counter 122, the reference month counter 113 and the reference day counter 114 are stored in the memory 104 through the corresponding input ports in the CPU 101, while the contents of the memory 104 are entered in the decoders 121 and 122 through the output ports PH0 to PH5 and PL0 to PL5 respectively.

The operation of the unit for use in an embodiment of the present invention will be described below by referring to Figs. 19 to 23.

When a power switch (not shown) is turned on, the CPU 101 is operated to run a program as shown in the flow chart in Fig. 22.

In Fig. 22, the CPU 101 starts to run the program from Step #01. Particularly, the CPU 101 calculates the number of passed days (PD) by subtracting the reference day (SD) from the current day stored in the memory 104 or the output from the current-day counter 109. On Step #02, the value (PD) is checked for positive or negative. If the value (PD) is positive, the number of passed months (PM) is determined on Step #06 by subtracting the output (SM) of the reference month counter

113 from the output (M) of the current-month counter 108. Then, the control proceeds to Step #07.

If the value (PD) is determined as negative on Step #02, the control proceeds to Step #03 where the number of days (DM) in the reference month ("29" as the number of days if the reference day is in a leap-year) is added to the calculated number of passed days (PD). Then, on Step #04, the number of passed months (PM) is calculated by subtracting the reference month (SM) from the current month (M). On Step #05, the number of passed month (PM) is reduced by 1 to offset the number of days (DM) in the reference month added to the number of passed days (PD). The, the control proceeds to Step #07.

On Step #07, the number of passed months (PM) is checked for positive or negative. If the value (PM) is positive, the control proceeds to Step #11 where the number of passed years (PY) is calculated by subtracting the reference year (SY) from the current year (Y), and to Step #12.

If the number of passed months (PM) is determined as negative on Step #07, the control proceeds to Step #08 where the number of passed months (PM) is incremented by 12, and to Step #09. On Step #09, as on Step #11, the number of passed years (PY) is calculated by subtracting the reference year (SY) from the current year (Y). On Step #10, as on Step #05, the number of passed years (PY) is reduced by 1. Then, the control proceeds to Step #12.

On Step #12, it is determined whether the number of passed years (PY) calculated on Step #10 or Step #11 is negative or not. If it is not negative, it means that the setting of the reference date is correct. On Step #13, the output of the output port WARN is kept on L level. On Step #14, it is checked if (PY) = 0 or not. If (PY) = 0, the control proceeds to Step #17. If (PY) ≠ 0, the control proceeds to Step #15. On Step #17, the number of passed months (PM) is outputted as the high-order digits (PH) of the time lapse display, while the number of passed days (PD) is outputted as the low-order digits (PL) of the time lapse display. On Step #19, the output of the YM/MD CTRL port in the CPU 101 is set to a "H" (high level). As the results, as shown in Fig. 23, the output terminal C0 of the decoder 123 is set to "L" (Low level), and the two other output terminals C1 and C2 are set to "H" (high level). Consequently, the segments in the unit display section 126 are excited in the form of "m" (month), while the segments in the unit display section 127 are excited in the form of "d" (day). Thus, the lapsed period of time "x months and x days" is displayed in the format of "x m" - "x d".

If the number of passed years is determined as (PY) ≠ 0 on Step #14, the instruction is given on Step #15 that the number of passed years (PY) and the number of passed months (PM) shall be displayed as the high-order digits (PH) and low-order digits (PL) of the

time lapse display respectively. On Step #18, the output level of the YM/MD CTRL port in the CPU 101 is set to "L" (low level). As the results, as shown in Fig. 23, the terminals C0 and C1 of the three output terminals on the decorder 123 are set to "H" (high level) in output level. Consequently, the segments in the unit display section 126 are lighted in the form of "y" (year), while the segments in the unit display section 127 are lighted in the form of "m" (month). Thus, the lapsed period of time "x years and x months" is displayed in the format of "x y" - "x m".

If it is determined on Step #12 that the number of passed years (PY) is negative, it means that the reference date is erroneously set as any date equal to or later than the current date. Then, the control proceeds directly to Step #16 where the output of the output port WARN is set to "H" (high level) to light the LED 131 through the driver circuit 130 in order to inform the user of the camera of the erroneous setting.

Carry-in and carry-out circuits are connected between the current-date counters 107 to 109. In addition, a day pulse produced by the day pulse generating circuit 106 is delivered to the current-day counter 109 every day. Therefore, the current-year counter 107, the current-month counter 108 and the current-day counter 109 are operated as a normal calendar to increment (advance) the current date as the time elapses and consequently to increment (vary) the time lapse display

as well.

Fig. 24 is a flow chart showing a partial modification of the flow chart as shown in Fig. 22, that is, a modification of the embodiment as shown in Fig. 19. In the flow chart in Fig. 22, the LED 131 is lighted to warn that the reference date is erroneously set as any date on or after the current date. In the embodiment as shown in Fig. 24, however, the display "Om Od" is provided essentially as the warning, if the status "O month and O day" occurs as shown on step #16' in Fig. 24. This procedure is run on Steps #12', #16', #17 and #19 in this order.

The remaining part of the flow chart in Fig. 24 is similar to that shown in the flow chart in Fig. 22. Therefore, the same step numbers are used for the same steps, and the description of the steps in this part of the flow chart as shown in Fig. 24 are omitted.

In this embodiment, it is understood that the lapsed period of time thus displayed can be imprinted on a film as sensitive means, as in the previous embodiment.

Reference is directed to our following co-pending Applications, wherein we have described and claimed various aspects of the cameras and devices described and claimed herein.

Application No.	Publication No.
88 09962.7	2,205,656
91	2
91	2
91	2
91	2

CLAIMS

1. A camera arranged for time-lapse photography, comprising:

(a) timer means for time-lapse photography; and

(b) prohibition means for prohibiting said timer means from operating when a camera main switch on the camera body is in the OFF state.

2. A camera according to claim 1, wherein there is provided:

(a) data-imprinting means for imprinting data on photosensitive means; and

(b) disabling means for disabling operation of said data-imprinting means should a shutter release operation be effected during a time-counting operation of said timer means.

3. An interval-photography device for a camera, comprising:

(a) timer means for time-lapse photography; and

(b) prohibition means for prohibiting said timer means from operating when a camera main switch on an associated camera body is in the OFF state.

4. A device according to claim 3, wherein there is provided:

(a) data-imprinting means for imprinting data on photosensitive means; and

(b) disabling means for disabling operation of

said data-imprinting means should a shutter release operation of an associated camera be effected during a time-counting operation of said timer means.

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